Morse Micro
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Bypass Boobytrap

APPNOTE-29

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1 Scope

This App Note applies to Morse Micro module reference designs incorporating an external power amplifier (PA) (e.g. MM6108-MF08651 Bailey_v13)

2 Introduction

High-frequency circuit performance is often influenced by unintended parasitic impedances, which can introduce variability in signal behavior across different boards. In RF designs, even minor variations in component tolerances, PCB layout, or assembly processes can lead to significant differences in circuit performance. Understanding these parasitic effects is critical to ensuring reliable and consistent operation.

This application note examines the impact of parasitic impedances in the MM6108-MF08651-US (Bailey 13.3) reference design, specifically within the front-end module (FEM). The observed variability in insertion loss and gain is attributed to components operating in their parasitic region, where impedance parameters are not well controlled. This uncontrolled behavior may lead to significant unit-to-unit variation. Through circuit modeling, simulation, and experimental validation, we analyze these effects and propose design modifications to improve performance consistency.

The findings of this study highlight the importance of accurately predicting and mitigating parasitic influences in high-frequency circuits. The methodologies presented here—modeling, simulation, and physical validation—provide a systematic approach for addressing similar design challenges in RF applications.

3 Parasitic Impedances

In electronic circuits, performance variability can arise from multiple sources, including noise, manufacturing tolerances, and parasitic effects inherent in the design and implementation of components. Understanding the cause of such variability is critical to ensuring reliable performance, especially in high-frequency and RF systems where small deviations can have significant effects.

This document investigates the root causes of variability observed in MM6108-MF08651-US (Bailey 13.3) reference design circuit, focusing on the role of parasitic impedances in key components. The observed variability manifests on a per-board basis, meaning that individual boards show consistent results when tested repeatedly, but performance differs between boards. This behavior suggests that the issue is not due to random noise but rather due to component tolerances or parasitic phenomena.

We aim to analyze the performance of this circuit by modeling and simulating potential sources of variation. By considering parasitic impedances and their effects on circuit performance, we can better understand the observed behavior and validate whether these effects align with experimental data. Ultimately, this analysis provides a foundation for explaining the circuit's performance and identifying strategies to mitigate variability.

Parasitic impedances are unintended electrical characteristics that arise due to the physical properties of components and circuit layouts. These parasitic effects are particularly significant in high-frequency circuits, where small inductive or capacitive elements can substantially alter the behavior of a design.

In real-world components, idealized behaviors are rarely achieved. For example:

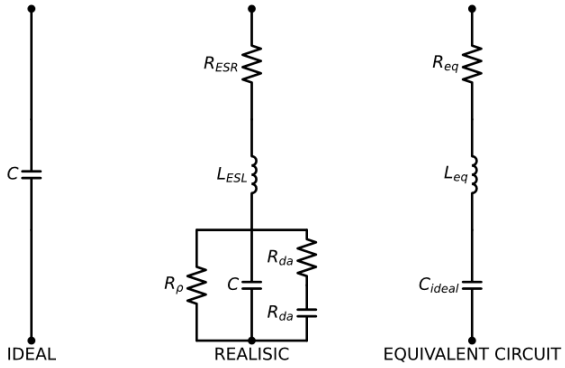
- Capacitors exhibit equivalent series inductance (ESL) and equivalent series resistance (ESR) due to their construction and materials.
- Inductors can have parasitic capacitances that affect their performance at higher frequencies.

The impact of these parasitics is magnified when operating in the RF range, where minor variations can lead to significant performance changes. These variations are influenced by:

1. **Manufacturing Tolerances:** Variability in the physical dimensions of components, which affect their electrical properties.
2. **Assembly Process:** Placement of components on the PCB, solder volume, and pad geometries, which can introduce additional parasitics.
3. **PCB Design:** Trace lengths, via placement, and layer stack-ups that contribute to overall impedance characteristics.

Example: Capacitor Parasitics

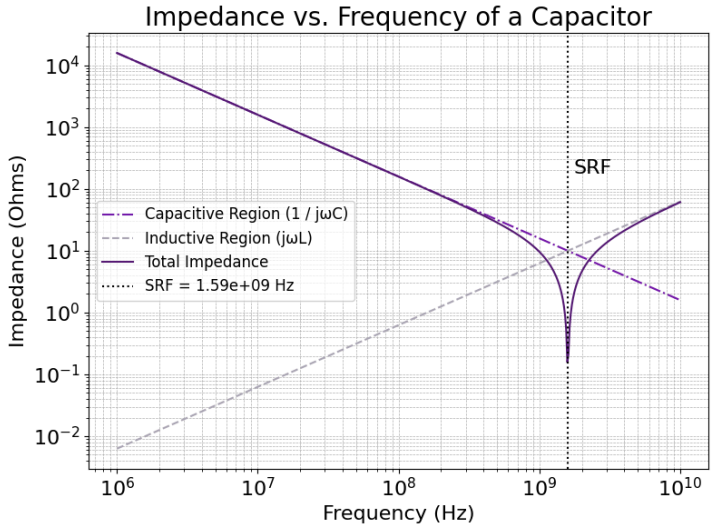
To illustrate, consider the behavior of capacitors. An ideal capacitor would exhibit a constant capacitance value. However, due to parasitic elements, its impedance varies with frequency, as shown in the following schematic model:



In this model:

- The nominal capacitance dominates at low frequencies.
- Parasitic inductance (ESL) becomes significant at higher frequencies, causing a self-resonant frequency (SRF).
- Beyond the SRF, the capacitor behaves inductively rather than capacitively.

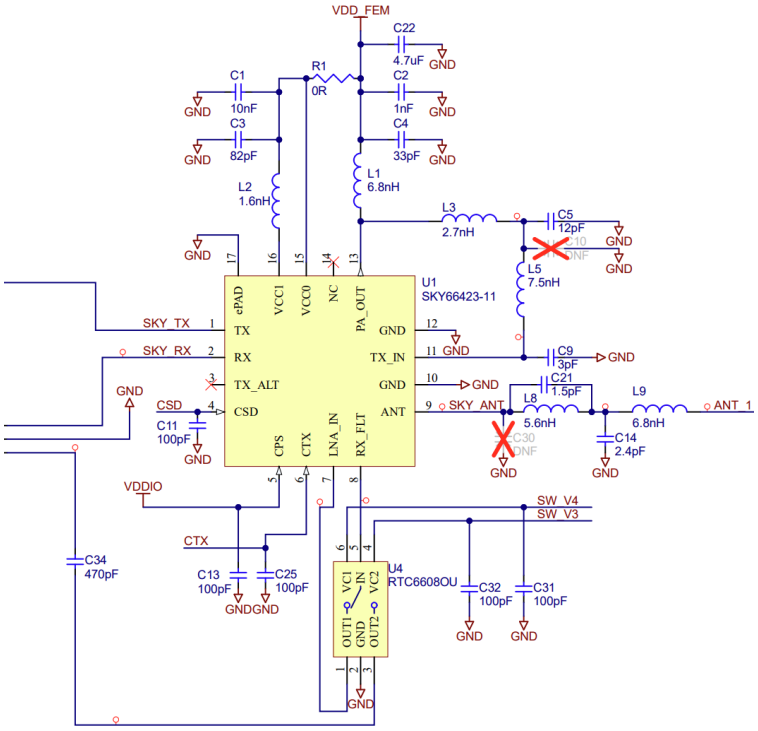
The following diagram demonstrates how a capacitor's impedance changes across frequencies, highlighting the self-resonant frequency and the transitions between capacitive and inductive behavior:



Such parasitic behaviors introduce variability in circuit performance.

4 Focus of this Analysis

Understanding parasitic effects in a general sense is essential for analyzing their potential impact on a specific circuit. In this investigation, the focus is on a front-end module (FEM) circuit containing capacitors, inductors, and an active device. The goal is to determine how parasitic elements, particularly in capacitors, could explain the variability observed across boards. To provide context, consider the following general schematic representation of the FEM section on the MM6108-MF08651-US (Bailey 13.3):



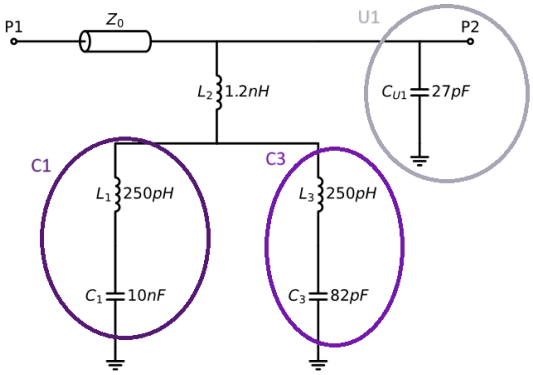
Parasitic Effects in the Front End Module

In the FEM circuit, we identify the following components and their potential parasitic contributions:

1. **C1 and C3:** Decoupling capacitors that exhibit parasitic inductance (ESL) and resistance (ESR). Initially we will only model ESL, but later we will see that ESR also plays an important role in this particular circuit. These parasitics influence the behavior of the circuit, particularly at higher frequencies where parasitic effects dominate.
2. **L2:** An inductor modeled as an ideal component for simplicity, as its parasitics are not suspected to contribute significantly to product performance variability.

3. **U1:** The active device, suspected to have internal capacitive behavior, particularly at the gate or input stage of its (hypothesized) internal transistor. While details of its implementation are not known, a capacitive model is believed to provide a reasonable approximation.

To better understand the role of these components and their parasitic contributions, a minimal circuit model was developed. This simplified representation isolates C1, L2, and C3 to focus on their combined effects on circuit behavior. By modeling these components with their associated parasitic elements, the interaction between the decoupling capacitors and the inductor can be analyzed, particularly at frequencies where parasitics dominate. The following diagram illustrates this minimal circuit:



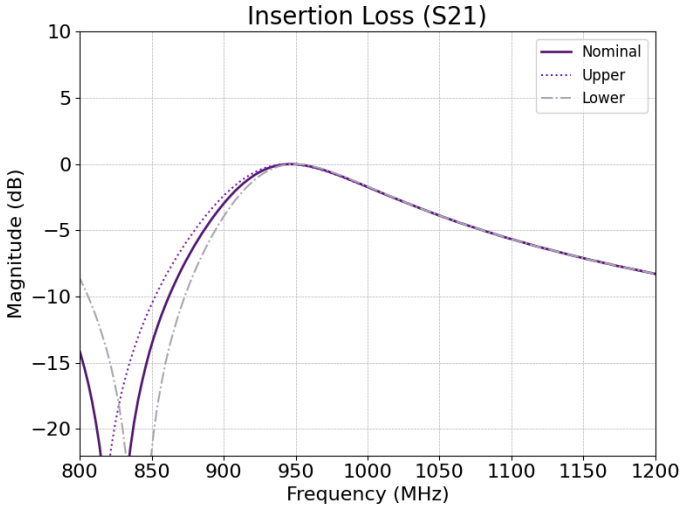
In this diagram, P1 represents the RF input (the SKY_TX net entering pin 1 of U1). We assume that pin 16 of U1 injects a bias onto the RF line and P2 represents the input to the main power amplifier transistor (the signal terminating here gets amplified to become the PA_OUT signal). The values of ESL (L_1 and L_3) were selected to approximate typical values found in 0201 component footprints.

5 Simulation

Simulating the Effect of Parasitic Variability

The value of a capacitor (e.g. 10nF) is a function of the geometry employed. It is affected by the dielectric constant of the material used along with the area and separation of its metallic plates. These parameters are generally tightly controlled in the manufacturing process. However, the value of the parasitic impedances is not controlled nor guaranteed by the manufacturer. We could expect large component to component variation if these parasitic tolerances were the culprit. Furthermore, the manufacturer is not their only source; for example, the placement of the component on its pads or amount of solder used could also affect the parasitic behaviour.

To model parasitic variability, we perform a Monte Carlo simulation that allows L_1 to fluctuate within 10% of its nominal value. We then measure the insertion loss between P1 and P2 to see how it may be affected.



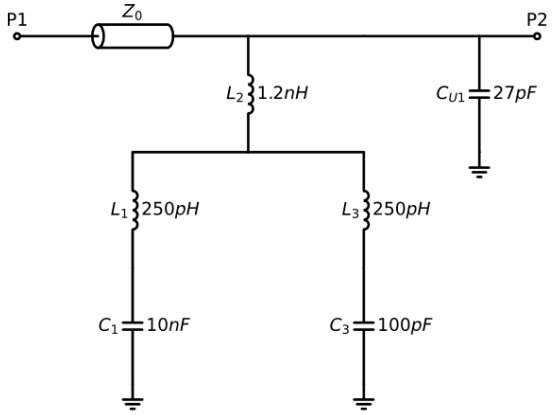
Measuring at 915MHz we can see the insertion loss vary between 0.9dB and 1.6dB. From this we can see that a 10% variation in the 250pH parasitic inductance in the 10uF capacitor is sufficient to explain a 0.7dB variation in gain!

The so-called ‘bypass boobytrap’ occurs due to the interaction between the smallest decoupling capacitor and the parasitic inductance of the second smallest decoupling capacitor. While this is a simplification—the actual resonance results from the combined influence of all components and parasitics—it highlights an unavoidable reality: a resonance will always exist somewhere. As designers, our responsibility is to predict its location and ensure it does not interfere with

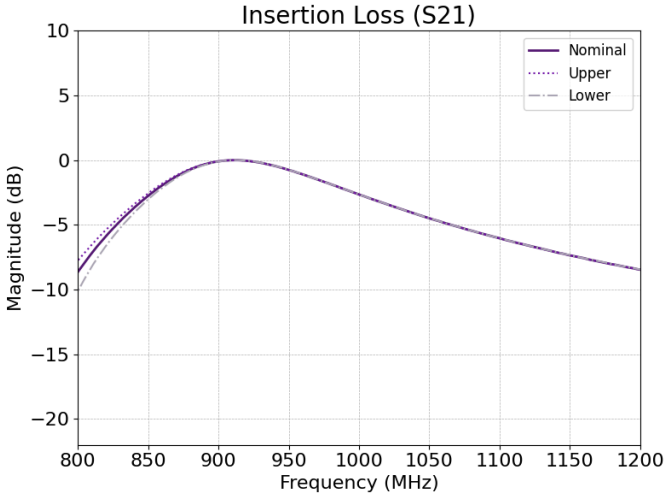
device operation, electromagnetic compatibility (EMC) requirements, or other critical considerations.

Simulating the Current Solution

It is well known that replacing the 82pF capacitor with a 100pF variant appears to resolve the issue—but why? An 18pF difference seems insignificant, especially compared to the adjacent 10nF capacitor. However, as our previous analysis has shown, this reasoning overlooks the impact of parasitic impedances. At higher frequencies, such as 900MHz, these parasitic effects become significant, making such assumptions unreliable. Lets update our schematic to match the new situation:



We now simulate our circuit and measure the insertion loss between P1 and P2, with L_1 still exhibiting a 10% variation:

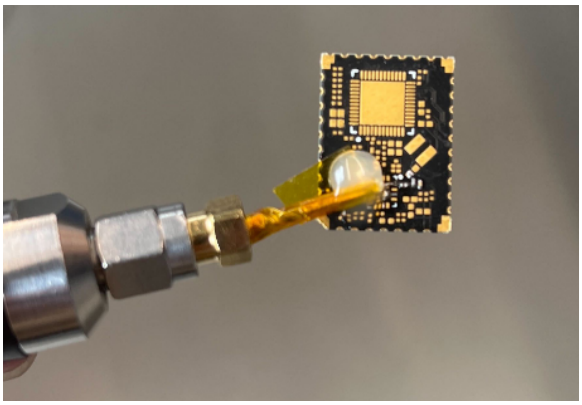


We have pushed the resonant frequency (resulting largely from the interaction between L_1 and C_3) from approximately 830MHz down to 770MHz. As a result, the variations caused by a 10% component tolerance are reduced to less than 0.1dB across the entire 902MHz to 928MHz range. Alternatively, changing C_1 from 0201 to 0402 would increase the value of L_1 and this would also shift the resonant frequency down by some amount. With 0201 component sizes, using C_3 = 100pF ensures consistent performance when the recommended components are used.

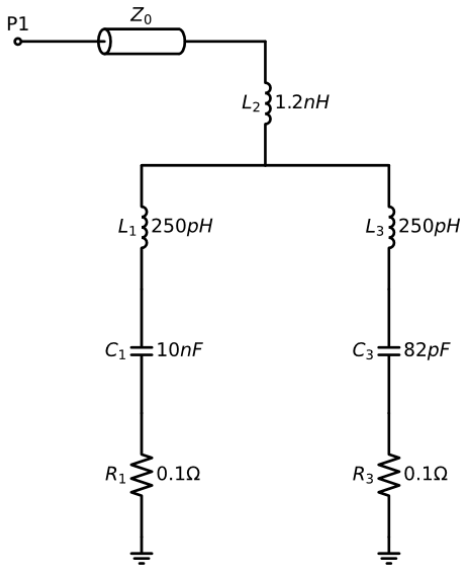
6 Testing

Testing the Current Solution

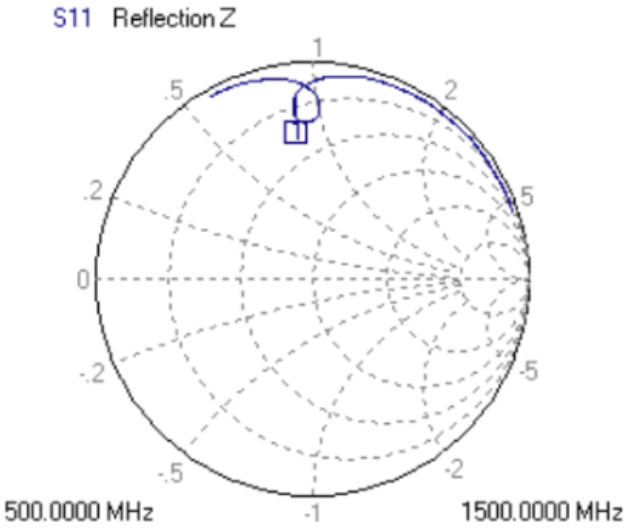
This all works very well in theory, but does it actually work? To evaluate the circuit's parasitic effects, we assembled a bare PCB with only C1, L2, and C3 intentionally omitting C22, C2, C4 and other secondary components. While these components contribute to the overall circuit behavior, their influence does not change the core finding: the variability issue is primarily driven by the resonance formed between C3 and the parasitic inductance of C1. This simplification allows for a direct comparison between empirical measurements and our simulation model, isolating the dominant source of variation.



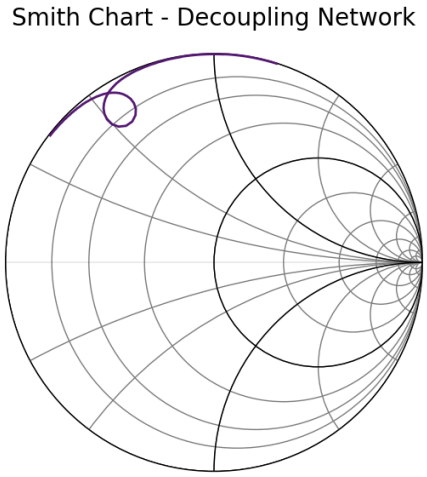
Updating our prior schematic model, we now need to remove U2 and apply ESR to C_1, and C_3 because now that we are using real components, they can no longer be neglected. For 0201 components, 100mΩ is a reasonable approximation.



Here a network analyser measurement of the impedance posed by our decoupling circuitry:



Here are the results of simulation of our schematic model:



By comparing the two graphs, we observe a dampened resonant peak in the 800 MHz to 900 MHz range, confirming that our schematic model captures the key factors influencing circuit behavior. This provides confidence in our approach. Further refining the simulation model to perfectly match the VNA measurement would be unproductive, as it would merely adjust parameters to fit a predetermined outcome rather than provide meaningful insight. Instead, with a viable simulation model in place, we have identified the critical components affecting performance and can anticipate their unintended parasitic behaviors. The model can only be truly validated by measuring actual component values and incorporating them into the simulation. This ensures the model reflects reality rather than simply being tuned to align with observations. Once validated, we can be confident that applying component modifications will resolve the issue, knowing exactly which elements to adjust and by how much. In the case of the MM6108-MF08651-US (Bailey 13.3) reference design, we have simulated and tested over a wide range of components and found component values that provide optimal performance when accounting for such parasitic interactions and component tolerance variations.

7 Conclusion

This analysis has demonstrated that parasitic impedances impact circuit performance in the MM6108-MF08651-US (Bailey 13.3) reference design. The observed performance variability across boards is primarily due to components operating in their parasitic region, where impedance parameters are not well controlled. Through circuit modeling, Monte Carlo simulations, and empirical validation, we have identified the critical role of the C3 decoupling capacitor in contributing to this uncontrolled variability.

By adjusting component values, specifically replacing C3 from an 82pF capacitor with a 100pF variant, the circuit shifts into an operating region where parasitic effects no longer cause significant performance variations. Simulation results indicate that this modification moves the resonance frequency outside the critical operating range, contributing to more consistent performance. Testing on physical hardware was used to validate these findings and reinforce the accuracy of the simulation model.

8 Revision History

Release Number	Release Date	Release Notes
01	10/01/2025	Initial Release

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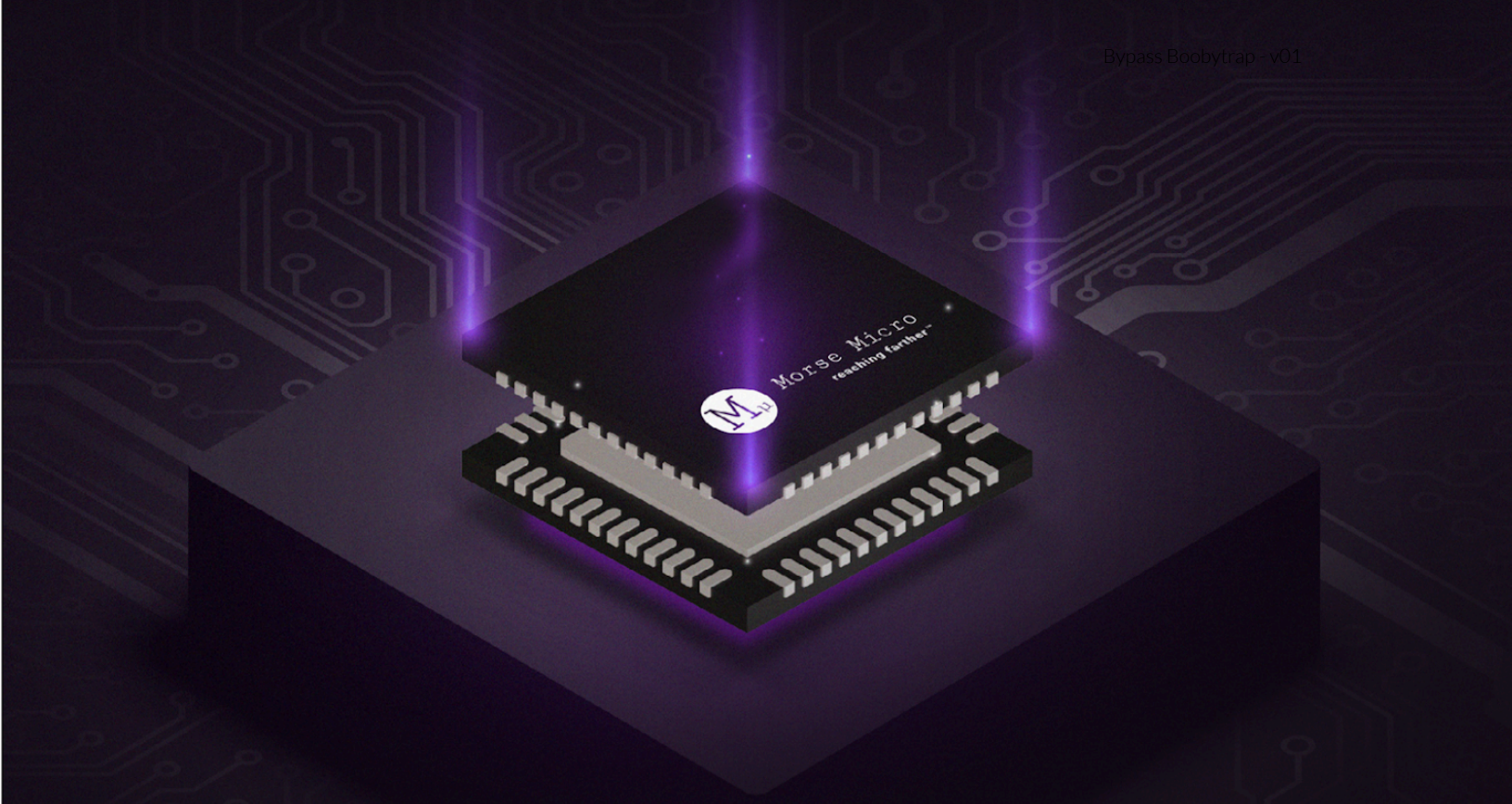
About Morse Micro

Morse Micro is producing IEEE 802.11ah / Wi-Fi HaLow solutions for Internet of Things (IOT) - based on a newly certified Wi-Fi standard called HaLow. Morse Micro is a VC-backed Startup headquartered in Sydney, Australia. Learn more at www.morsemicro.com



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