



MM8108 SoC Data Sheet

Multi-region Wi-Fi HaLow/IEEE 802.11ah
Sub-1 GHz SoC with USB Interface and
Integrated Power and Low Noise Amplifiers



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1 Product Overview

1.1 Introduction

Wi-Fi HaLow (pronounced "HEY-low") is the first global Wi-Fi standard (IEEE 802.11ah) specifically designed to meet the needs of the Internet of Things (IoT). It's an open standard wireless network technology operating in the sub-1 GHz license-exempt RF bands (850 MHz to 950 MHz range), so it doesn't incur ongoing monthly costs like cellular/mobile network connections. By operating in the sub-1 GHz range, this low-power wireless protocol can connect more IoT devices over much longer distances and with significantly lower power consumption than traditional Wi-Fi.

Morse Micro, the world's leading Wi-Fi HaLow solutions provider, offers several Wi-Fi HaLow connectivity solutions. The MM8108 SoC is a single-chip solution that incorporates radio, PHY, and MAC functions, all of which are compliant with the IEEE 802.11ah standard. It supports world-leading power efficiency and PHY rates up to 43.3 Mbps using world-first 256-QAM modulation at an 8 MHz bandwidth. It is ideal for power-sensitive and high-speed applications.

Its integrated power amplifier (PA) offers world-leading transmit performance and energy efficiency with on-chip amplification of up to 26 dBm, which is ideal for low-cost devices. For ultra-long reach applications, the MM8108 can be paired with an external PCB mount power amplifier, typically included in front-end modules (FEMs).

The high-performance integrated low-noise amplifier (LNA) offers exceptional receive sensitivity.

These features, combined with digital transmit filtering and pre-distortion circuits, result in an advanced transceiver design that ensures out-of-the-box compatibility with all global Wi-Fi HaLow regulatory environments while reducing external component costs by eliminating the requirement for expensive external filters.

MM8108 supports a USB 2.0 High-Speed host interface and an SDIO/SPI host interface, offering solution architects flexibility when integrating Wi-Fi HaLow connectivity into their existing solution.

With a footprint of only 5 mm x 5 mm and a higher level of integration than previous generations of chipsets, the MM8108 can fit even smaller designs while substantially reducing the overall cost of materials.

MM8108 supports WPA3 and all standard security features required for Wi-Fi HaLow product certifications.

1.2 Features

- Single-stream maximum PHY rate of 43.3 Mbps at 8 MHz bandwidth
- Radio supporting all global Sub-1 GHz frequency bands
 - Frequency Range: 850 MHz to 950 MHz
 - Channel width options of 1/2/4/8 MHz
 - High power and extremely high efficiency integrated PA with maximum 26 dBm (400 mW) output power at 45% PA efficiency and 37% SoC efficiency
 - Novel PA architecture maintains efficiency at power backoff
 - Low-power receiver with integrated LNA, NF < 4 dB
 - Compatible with external LNA, PA for higher power or sensitivity requirements
- 802.11ah OFDM PHY with Wi-Fi Alliance Wi-Fi HaLow certification
 - BPSK, QPSK, 16-QAM, 64-QAM and 256-QAM
 - Automatic frequency and gain control
 - Packet detection and channel equalization
 - Forward Error Correction (FEC) coding and decoding
 - Modulation and Coding Scheme (MCS) levels 0-10
 - 1 MHz duplicate mode
 - Optional traveling pilots
- 802.11ah MAC with Wi-Fi Alliance Wi-Fi HaLow certification
 - Support for Station (STA) and Access Point (AP) roles
 - Listen-Before-Talk (LBT) access with energy detection
 - 802.11 power save
 - 802.11 fragmentation and defragmentation
 - Power-Saving Target Wake Time (TWT) support for extended battery life
 - Automatic and manual MCS rate selection
- On-chip software stack assisting with host offload of Wi-Fi connection management
- USB 2.0 High-Speed compliant device interface
 - Integrated USB 2.0 PHY and device interface supporting High-Speed mode at 480 Mbps
- SDIO 2.0 compliant device interface
 - SDIO 2.0 High-Speed at 50 MHz max for 200 Mbps
 - Support for 1-bit and 4-bit data mode
 - Support for SPI mode operation at up to 80 MHz for 80 Mbps

- Power Management Unit (PMU) supporting various modes of operation
 - Single supply 3.0-3.6 V for integrated DC-DCs and LDOs
 - Multiple low-power modes (hibernate, deep sleep, snooze, USB snooze) support extreme power environments
 - Support for an external real-time clock source providing the highest accuracy timing for sleep modes
- Wide spectrum of security features
 - Wi-Fi layer security, including Wi-Fi Protected Access version 3 (WPA3), Protected Management Frames (PMF), and Opportunistic Wireless Encryption (OWE)
 - Hardware support for Advanced Encryption Standard (AES) and Secure Hash Algorithm version 2 (SHA-2) functions (SHA-256, SHA-384, SHA-512)

1.3 Applications

For Internet of Things (IoT) and Machine-to-Machine (M2M) applications, such as:

- Surveillance Cameras and Sensors
- Cloud Connectivity
- Low-power Sensor Networks
- Building Automation Systems
- Asset Tracking and Management
- Machine Performance Monitors and Sensors
- Building Access Control and Security
- Drone Video and Navigation Communications
- Connected Toys and Games
- Rural Internet Access
- Agricultural Networks
- Utility Smart Meter and Intelligent Grid
- Proximity Sensors
- Industrial Automation Controls
- Smart Home Automation
- EV Car Chargers
- Appliances
- Construction Site Connectivity
- Smart Signs and Kiosks
- Retail Point-of-Sale Terminals
- Vehicle-to-Vehicle Communications
- IP Sensor Networks
- Biometric IDs and Keypads
- Warehouse Connectivity
- Intelligent Lighting Controls
- BT/ZigBee™/Z-Wave™ to Wi-Fi HaLow Gateways
- Smart City Networks

2 Pin Overview

2.1 Pin Layout

The MM8108 device package features 79 pins in a 5 mm x 5 mm package, as described in this section.

	1	2	3	4	5	6	7	8	9	
A	GND	XON	XOP	GND	VBUCK	WAKE_UP	VBUCK_FB	VBAT_PWR	GND	A
B	RTC_XON	NC	NC	VBUCK	VBAT_AON	RESET_N	GND	GND	VSW	B
C	RTC_XOP	NC	NC	NC	GND	GPAIO	NC	GND	GND	C
D	GND	GND	LO_TEST	GND	GPIO_12	JTAG_TMS	JTAG_TDO	SDIO_D3	SDIO_D0	D
E	RFIN	GND	NC	GPIO_9	GPIO_11	JTAG_TCK	JTAG_TDI	SDIO_D2	SDIO_D1	E
F	GND	Depopulated	GND	GPIO_8	GPIO_10	GND	GND	SDIO_CMD	SDIO_CLK	F
G	RF_OUT	Depopulated	VBUCK_TX	GPIO_7	GPIO_3	GPIO_4	GPIO_5	VDDIO	GND	G
H	GND	VBUCK_TX	GPIO_6	GPIO0	GPIO_1	GPIO_2	GND	GND	VSW_TX	H
J	GND	VBUCK_TX	GND	USB_DP	USB_DM	USB_VCC33A	VBUCK_FB_TX	VBAT_PWR_TX	GND	J
	1	2	3	4	5	6	7	8	9	

Ball category

- Analog signals
- Digital signals on VDDIO
- Supply/ground
- USB signals
- Not connected
- Depopulated

Figure 1: Pin diagram

2.2 Pin Descriptions

The two buck converters on MM8108 are referred to as BUCK and BUCK_TX, which have output voltages of 1.2 V and 1.8 V, respectively.

Pin	Default Functionality			Alternative 1	Alternative 2
	Pin Name	Type	Description	Pin Name	Pin Name
A1	GND	Ground			
A2	XON	Analog	32 MHz crystal connection		
A3	XOP	Analog	32 MHz crystal connection		
A4	GND	Ground			
A5	VBUCK	Supply	BUCK voltage		
A6	WAKE_UP	Analog	External wake from Deep Sleep and Snooze		
A7	VBUCK_FB	Supply	Voltage sense pin for BUCK output		
A8	VBAT_PWR	Supply	3.3 V VBAT supply for BUCK		
A9	GND	Ground			
B1	RTC_XON	Analog	RTC XTAL connection, NC if unused		
B2	NC	Not connected			
B3	NC	Not connected			
B4	VBUCK	Supply	BUCK output voltage		
B5	VBAT_AON	Supply	3.3 V VBAT supply for the AON unit		
B6	RESET_N	Analog	Asynchronous chip reset (active low)		
B7	GND	Ground			
B8	GND	Ground			
B9	VSW	Supply	BUCK switching node		
C1	RTC_XOP	Analog	RTC XTAL connection, NC if unused		
C2	NC	Not connected			
C3	NC	Not connected			
C4	NC	Not connected			
C5	GND	Ground			
C6	GPAIO	Analog	Analog test signal (keep grounded)		
C7	NC	Not connected			

Pin	Default Functionality			Alternative 1	Alternative 2
	Pin Name	Type	Description	Pin Name	Pin Name
C8	GND	Ground			
C9	GND	Ground			
D1	GND	Ground			
D2	GND	Ground			
D3	LO_TEST	Analog	Analog test signal (keep grounded)		
D4	GND	Ground			
D5	GPIO_12	Digital I/O		FEM_Control	FEM_Control
D6	JTAG_TMS	Digital I/O	JTAG mode select		
D7	JTAG_TDO	Digital I/O	JTAG data out		
D8	SDIO_D3	Digital I/O	SDIO/SPI data line	SPI_CS	QSPI_D3
D9	SDIO_D0	Digital I/O	SDIO/SPI data line	SPI_MISO	QSPI_D0
E1	RFIN	RF	Receiver input		
E2	GND	Ground			
E3	NC	Not connected		QSPI_CSB_1	QSPI_CSB_1
E4	GPIO_9	Digital I/O			
E5	GPIO_11	Digital I/O		FEM_Control	FEM_Control
E6	JTAG_TCK	Digital I/O	JTAG clock		
E7	JTAG_TDI	Digital I/O	JTAG data in		
E8	SDIO_D2	Digital I/O	SDIO/SPI data line	47 k Ω pull-up needed	QSPI_D2
E9	SDIO_D1	Digital I/O	SDIO/SPI data line	SPI_IRQ	QSPI_D1
F1	GND	Ground			
F2	Depopulated				
F3	GND	Ground			
F4	GPIO_8	Digital I/O		BUSY	BUSY
F5	GPIO_10	Digital I/O		FEM_Control	FEM_Control
F6	GND	Ground			
F7	GND	Ground			
F8	SDIO_CMD	Digital I/O	SDIO/SPI command/data line	SPI_MOSI	QSPI_CSB
F9	SDIO_CLK	Digital I/O	SDIO/SPI clock input	SPI_SCK	QSPI_CLK
G1	RF_OUT	RF	Transmitter output		
G2	Depopulated				
G3	VBUCK_TX	Supply	BUCK_TX voltage for the transmitter		
G4	GPIO_7	Digital I/O		DBG_UART_MM_RX	DBG_UART_MM_RX
G5	GPIO_3	Digital I/O		QSPI_D1	UART_RX
G6	GPIO_4	Digital I/O		QSPI_D2	UART_RTS
G7	GPIO_5	Digital I/O		QSPI_D3	UART_CTS

Pin	Default Functionality			Alternative 1	Alternative 2
	Pin Name	Type	Description	Pin Name	Pin Name
G8	VDDIO	Power	Host supply for digital I/O		
G9	GND	Ground			
H1	GND	Ground			
H2	VBUCK_TX	Supply	BUCK_TX voltage for the transmitter		
H3	GPIO_6	Digital I/O		DBG_UART_MM_TX	DBG_UART_MM_TX
H4	GPIO_0	Digital I/O		QSPI_CLK	
H5	GPIO_1	Digital I/O		QSPI_CSB_0	
H6	BUSY	Digital I/O	BUSY signal output	QSPI_D0	UART_TX
H7	GND	Ground			
H8	GND	Ground			
H9	VSW_TX	Supply	BUCK_TX switching node		
J1	GND	Ground			
J2	VBUCK_TX	Supply	BUCK_TX voltage for the transmitter		
J3	GND	Ground			
J4	USB_DP	USB I/O	USB Data Plus (DP) line		
J5	USB_DM	USB I/O	USB Data Minus (DM) line		
J6	USB_VCC33A	Supply	USB 3.3 V supply		
J7	VBUCK_FB_TX	Supply	Voltage sense pin for BUCK_TX		
J8	VBAT_PWR_TX	Supply	3.3V VBAT supply to BUCK_TX		
J9	GND	Ground			

Table 1: Pin description

Alternative Pin Functionality Descriptions	
Pin Name	Description
FEM_Control	External front-end module control
SPI_SCK	SPI host interface serial clock
SPI_MOSI	SPI host interface master out, slave in
SPI_MISO	SPI host interface master in, slave out
SPI_IRQ	SPI host interface interrupt line
SPI_CS	SPI host interface chip select
QSPI_CLK	QSPI interface clock
QSPI_D0	QSPI interface data line 0
QSPI_D1	QSPI interface data line 1
QSPI_D2	QSPI interface data line 2
QSPI_D3	QSPI interface data line 3
QSPI_CSB_0	QSPI interface chip select device 0
QSPI_CSB_1	QSPI interface chip select device 1
BUSY	Busy signal output
DBG_UART_MM_RX	Debug UART receive data
DBG_UART_MM_TX	Debug UART transmit data
UART_RX	UART host interface receive data
UART_TX	UART host interface transmit data
UART_RTS	UART host interface request to send
UART_CTS	UART host interface clear to send

Table 2: Alternative pin functionality description

3 Functional Description

The following sections describe the functions of the MM8108 device.

3.1 Functional Block Diagram

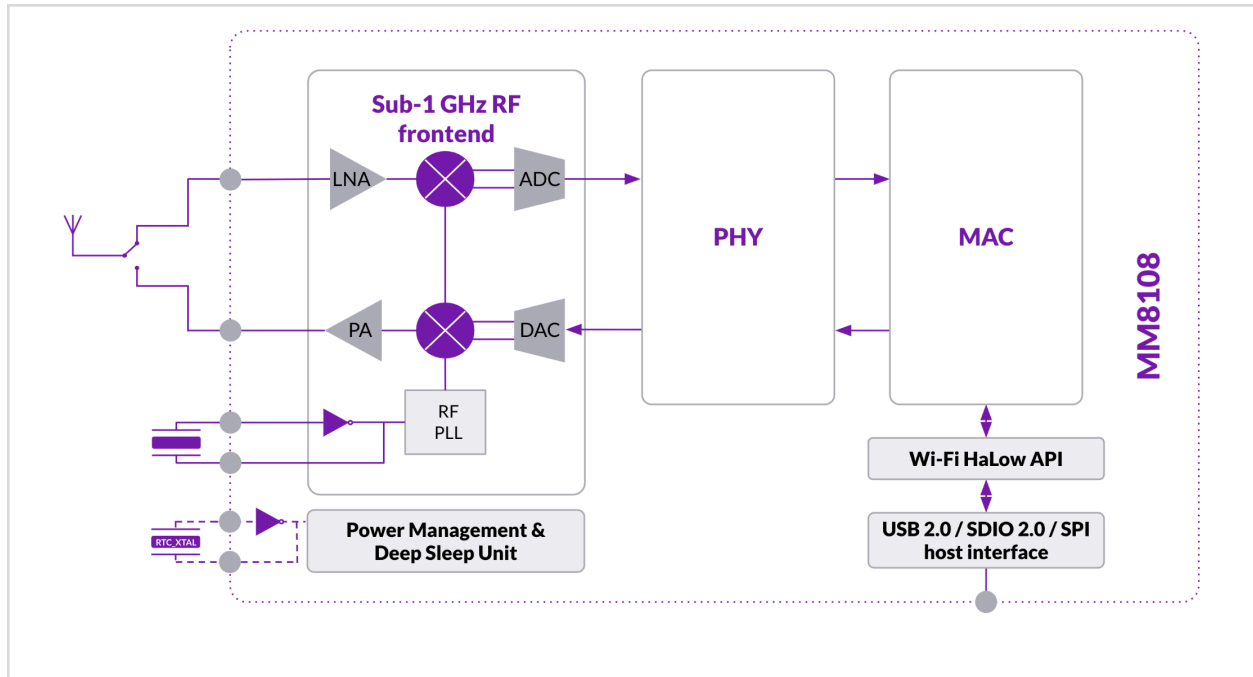


Figure 2: Functional block diagram

3.2 Clocks

3.2.1 XTAL Clock

Deriving clocks in the RF and digital subsystems requires a 32 MHz crystal (XTAL) component. As shown in Figure 3, a Pierce oscillator circuit is used.

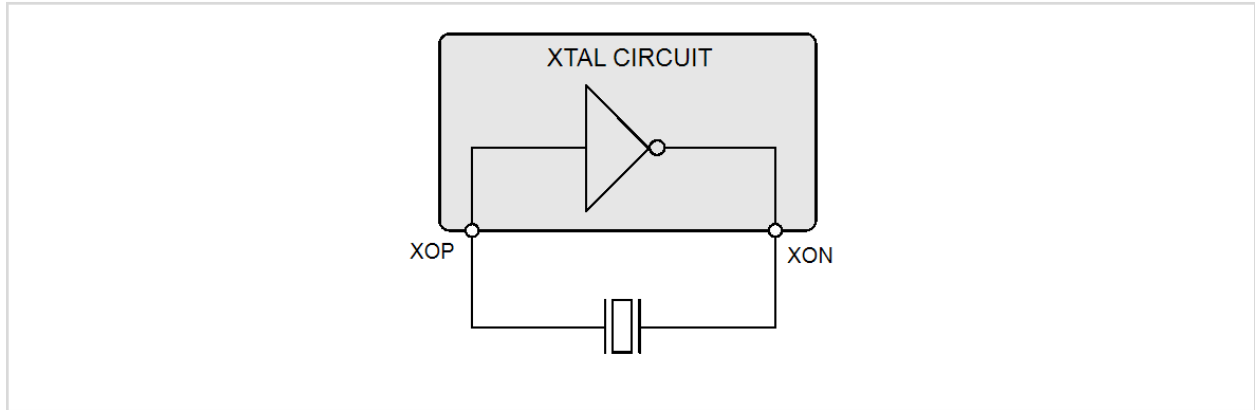


Figure 3: Crystal circuit

The crystal is connected between pins XOP & XON. The crystal load capacitance and driver is provided internally inside the chip (denoted in the gray box above). No external load capacitors are required on the PCB.

The crystal component should meet the following specifications across the expected temperature range of operation to comply with 802.11ah standards for frequency offset and achieve the specified sensitivity.

XTAL Specifications	Min	Typ	Max	Units
Frequency tolerance	-	-	20	ppm
ESR	10	-	100	Ω
Load capacitance	-	8	-	pF

Table 3: Crystal component specification

Note: The crystal component frequency tolerance above is without trimming and is across temperature for the component's lifetime. The equipment designer is responsible for selecting a crystal component that complies with these specifications.

3.2.2 RTC XTAL Clock

A 32.768 kHz crystal driver circuit is available for optional use as a real-time clock (RTC) source. This source provides the highest accuracy timing for system sleep modes compared with the on-chip RC oscillator, which is used if an RTC XTAL is absent.

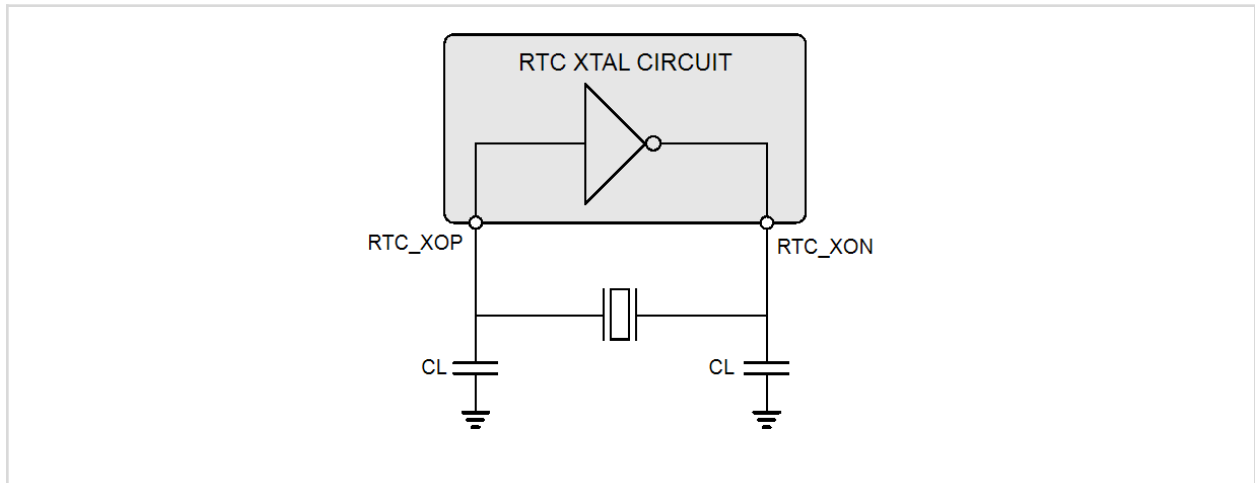


Figure 4: RTC crystal circuit

As shown in Figure 4, the crystal should be connected between pins RTC_XOP and RTC_XON. Load capacitors CL must be placed at these pins and coupled to Ground. The capacitance values should follow the suggestions of the crystal datasheet. The crystal stability should be +/-30 ppm or better for accurate sleep time control.

RTC XTAL Specifications	Min	Typ	Max	Units
Frequency tolerance	-	-	30	ppm
ESR	-	90	-	kΩ
Load capacitance	-	12.5	-	pF

Table 4: RTC crystal component specification

3.3 Power Management

3.3.1 Power Supply

All power is derived from a 3.0 V to 3.6 V power source connected to VBAT_PWR (A8), VBAT_AON (B5), and VBAT_PWR_TX (J8).

VDDIO (G8) can be connected to the same 3.0 V to 3.6 V power source or, if available, to the host's dedicated VDDIO rail.

For optimal performance, 4.7 uF, 470 nF, 10 uF, and 470 nF decoupling capacitors are required at VBAT (A8), VBAT_AON (B5), VBAT_PWR_TX (J8), and VDDIO (G8), respectively.

VSW (B9) requires a 2.2 uH/10 uF LC filter and a 4.7 uF decoupling capacitor at VBUCK (A5, B4). The VBUCK_FB (A7) feedback connection must be as close as possible to the load pin VBUCK (A5, B4).

VSW_TX (H9) requires a 1.5 uH/22 uF LC filter at VBUCK_TX (G3, H2, J2). The VBUCK_TX_FB (J7) feedback connection must be as close as possible to the load pin VBUCK_TX (G3, H2, J2).

All ground pins should be connected to a solid ground plane on the second layer of the PCB.

3.3.2 Power Modes

An internal Power Management Unit (PMU) provides multiple low-power modes that the chip may enter via firmware routines.

Power Mode	Wake From				1 MB SRAM Retained
	RESET_N (B6)	WAKE_UP (A6)	Internal Timer	USB Signalling	
Hibernate	Yes	No	No	No	No
Deep Sleep	Yes	Yes	Yes	No	No
Snooze	Yes	Yes	Yes	No	Yes
USB snooze	Yes	Yes	Yes	Yes	Yes

Table 5: Power modes overview

Note:

- Using RESET_N (B6) to wake the chip will cause a complete chip reboot with no retention of any kind of memory

3.3.2.1 Hibernate

Hibernate mode draws the least current of the low-power modes. It may be exited only by toggling the RESET_N (B6) pin, which causes the chip to reboot.

While in hibernate mode, the chip will not respond to the WAKE_UP (A6) pin or run an internal timer, and no internal memory will be retained.

3.3.2.2 Deep Sleep

Deep Sleep mode can be exited by toggling the RESET_N (B6) pin, which causes a complete chip reboot, asserting the WAKE_UP (A6) pin, or by using an internal timer (running on the real-time clock source).

While in Deep Sleep mode, no internal memory will be retained.

3.3.2.3 Snooze

Snooze mode can be exited by toggling the RESET_N (B6) pin, which causes a complete chip reboot, by asserting the WAKE_UP (A6) pin, or by using an internal timer (running on the real-time clock source).

If the chip resumes operation via the WAKE_UP (A6) pin or an internal timer, 1 MB of SRAM memory will be retained.

No internal memory will be retained if the chip is rebooted using the RESET_N (B6) pin.

3.3.2.4 USB Snooze

USB snooze mode can be exited by toggling the RESET_N (B6) pin, which causes a complete chip reboot by asserting the WAKE_UP (A6) pin, using an internal timer (running on the real-time clock source), or by resuming signaling over the USB bus from the USB host.

If the chip resumes operation via the WAKE_UP (A6) pin, an internal timer, or USB resume signaling, 1 MB of SRAM memory will be retained.

No internal memory will be retained if the chip is rebooted using the RESET_N (B6) pin.

3.4 Boot/Reset Sequencing

3.4.1 Boot Timing

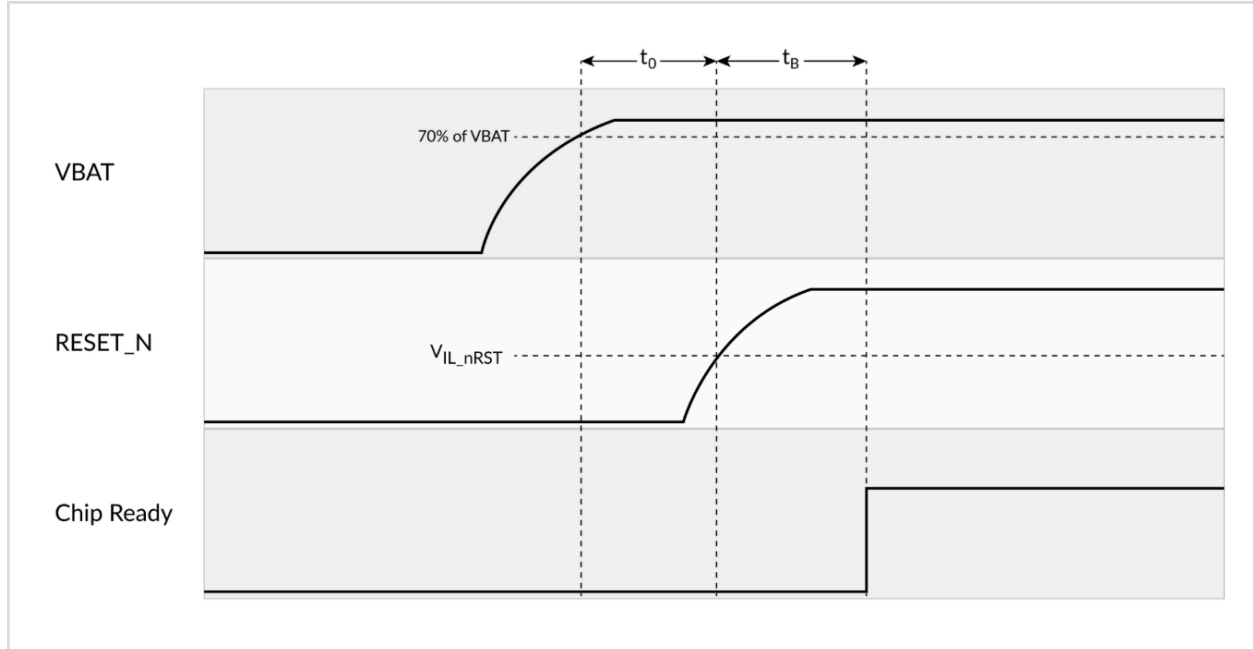


Figure 5: Boot timing diagram

Parameters	Description	Min	Max	Unit
V_{IL_nRST}	Reset threshold	450	-	mV
t_0	Time between VBAT brought up (3.3 V) and RESET_N being activated	50	-	μs
t_B	Boot time	-	10	ms

Table 6: Boot timing overview

3.4.2 Reset Timing

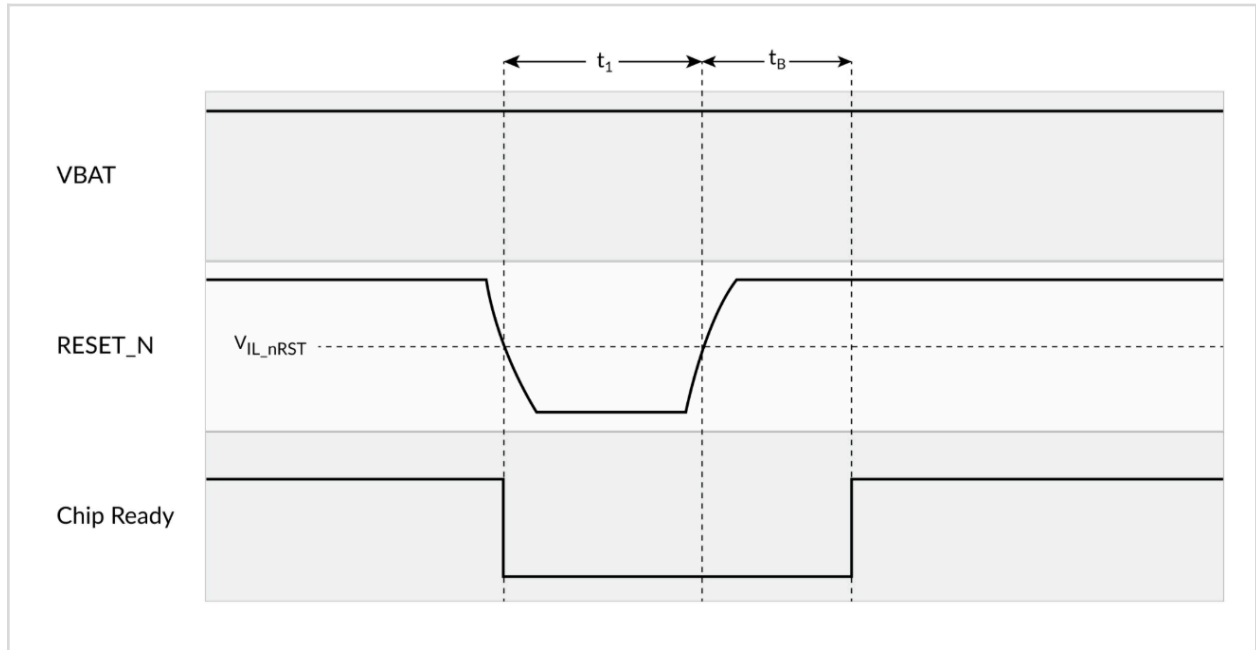


Figure 6: Reset timing diagram

Parameters	Description	Min	Max	Unit
V_{IL_nRST}	Reset threshold	450	-	mV
t_1	Duration of RESET_N signal level $< V_{IL_nRST}$ to reset the chip	1	-	ms
t_B	Boot time	-	10	ms

Table 7: Reset timing overview

3.4.3 Low-Power Modes

Exiting any low-power mode takes at most 10 ms.

3.5 USB Host Interface

A USB 2.0 High-Speed host interface is available, supporting device mode only at up to 480 Mbps.

3.5.1 Pin Description

Pin	Pin Name	Description
J4	USB_DP	High-speed differential pin, DP
J5	USB_DM	High-speed differential pin, DM
J6	USB_VCC33A	3.3 V analog supply voltage for USB 2.0

Table 8: USB bus pins

3.5.2 Features

- An integrated USB 2.0 PHY and MAC capable of up to High-Speed mode at 480 Mbps
- Device endpoints implementing bulk data, isochronous transfers, and interrupts for the USB host driver to operate the chip as a network AP or STA
- Suspend and resume power management functions
- USB snooze mode with in-band wake
- The USB link must be suspended to enter USB snooze mode.
- The chip will initiate wake from USB snooze mode and return to normal operation mode when the USB host issues resume signaling over the USB bus (in-band).

Parameter	Min	Typ	Max	Unit
USB_VCC33A	3.0	3.3	3.6	V
V_{noise_33A} (Allowable power noise on supply, 1 Hz-100 kHz)	-	-	150	mV
I_{VCC33A}	-	8.1	8.4	mA

Table 9: USB bus electrical specifications

3.6 SDIO Host Interface

A host interface is available via SDIO 2.0, capable of High-Speed mode and operating at 3.3 V.

3.6.1 Pins

Pin	Pin Name	SDIO 4-bit Mode	SDIO 1-bit Mode
F9	SDIO_CLK	Clock pin (input)	
F8	SDIO_CMD	Command pin	
D9	SDIO_D0	Data pin 0	
E9	SDIO_D1	Data pin 1	IRQ
E8	SDIO_D2	Data pin 2	Unused
D8	SDIO_D3	Data pin 3	Unused

Table 10: SDIO pins

3.6.2 Bus Timing

The SDIO clock rate supports up to 50 MHz. The SDIO bus always operates in High-Speed (25 Mbps) mode.

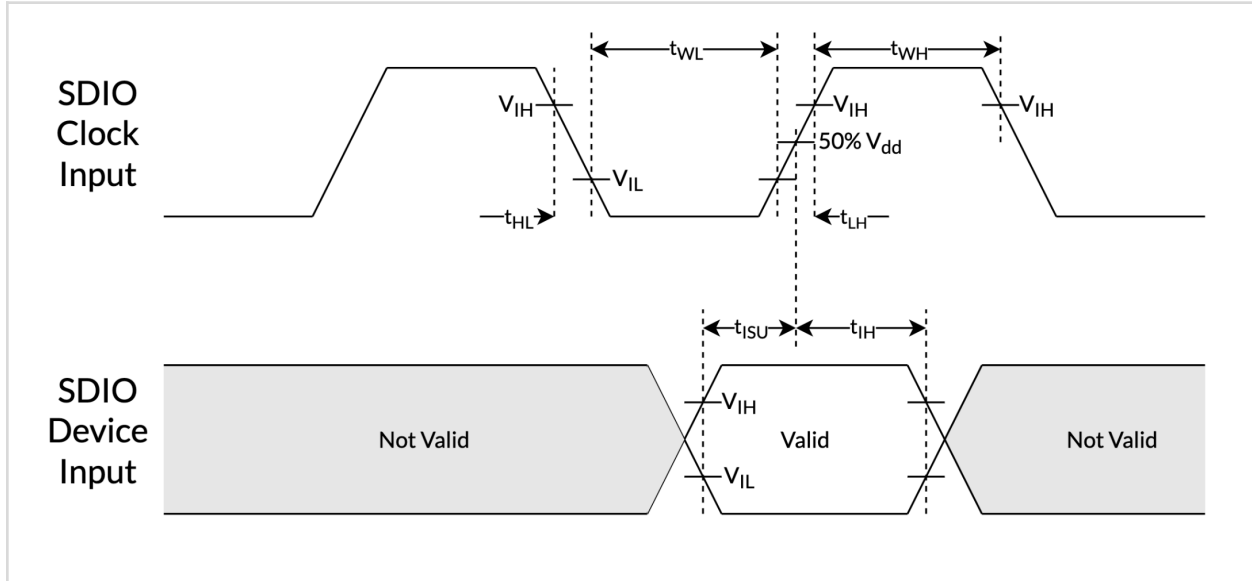


Figure 7: SDIO device bus input timing diagram

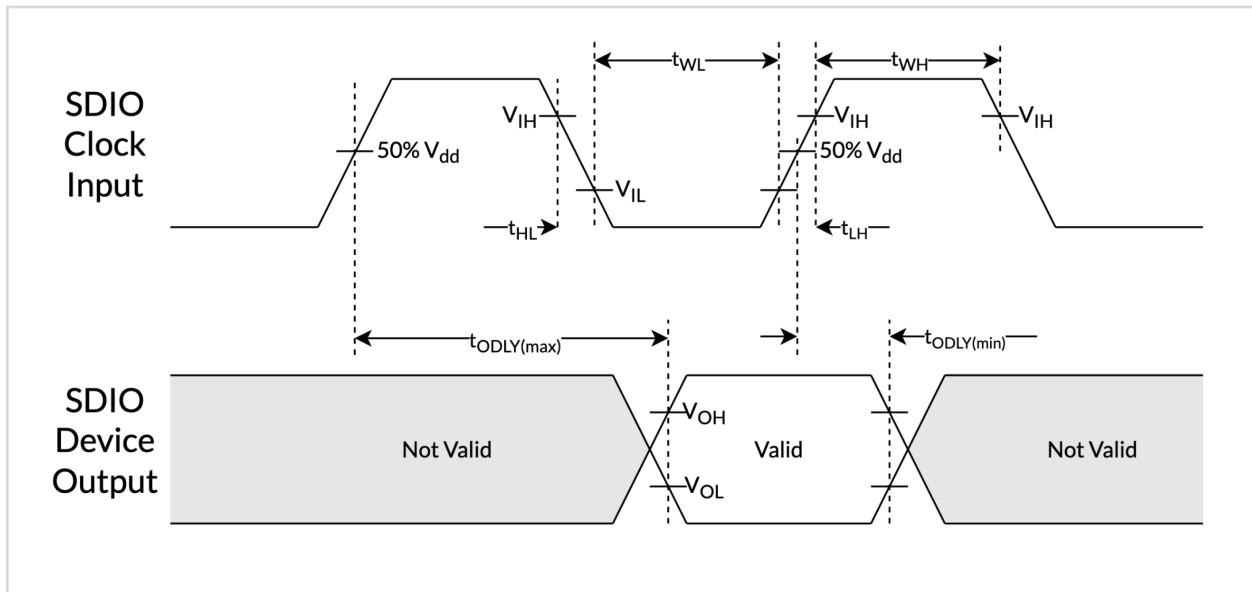


Figure 8: SDIO device bus output timing diagram

Parameter	Min	Max	Units
Clock frequency	0	50	MHz
Clock low time (t_{WL})	7	-	ns
Clock high time (t_{WH})	7	-	ns
Clock rise time (t_{LH})	-	3	ns
Clock fall time (t_{HL})	-	3	ns
Input setup time (t_{ISU})	6	-	ns
Input hold time (t_{IH})	2	-	ns
Output delay ($t_{ODLY(max)}$)	-	14	ns
Output hold time ($t_{ODLY(min)}$)	2.5	-	ns
Total system capacitance for each line	-	40	pF

Table 11: SDIO bus timing

3.7 SPI Host Interface

The SPI interface uses the pin layout as defined below, over which the modified SDIO protocol is used for communication.

3.7.1 Pins

Pin	Pin Name	SPI mode function
D8	CS	Chip select (active low)
E9	INT	Interrupt pin
D9	MISO	Master data in/slave data out
F8	MOSI	Master data out/slave data in
F9	CLK	Clock pin (input)
E8	Unused	Unused, needs to be pulled high for SPI mode

Table 12: SPI bus pins

3.7.2 Initialization in SPI Mode

After power-on, the host interface can be brought up as either SDIO or SPI. Per the SDIO specification, the host must send a CMD0 while holding CS low (its asserted state) to switch the interface to SPI mode.

For further details on the protocol, refer to the SD Specification Part E1 “SDIO Simplified Specification” version 2.00.

3.7.3 SPI Bus Timing

The SPI clock rate supports up to 80 MHz. The SPI bus timing is identical to the SDIO bus timing, including considering MOSI and MISO as input and output timing, respectively.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO High-Speed mode. After being initialized, the SPI bus may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge).

3.8 GPIO

3.8.1 Features

Up to 12 programmable General Purpose Input/Output (GPIO) pins are available.

Each pin can be configured with a unique drive value and with driving enabled or disabled. The value of each pin can be read whether driving or not.

Each pin can be configured to generate an interrupt based on level or edge (rising or falling). Inputs are synchronized to the main digital clock, so any pulses must be at least 31.25 us in length.

There are internal pull-up and pull-down facilities in the pads and drive-strength selection.

3.8.2 Reset State

GPIO pins will be undriven at boot and in a high impedance state.

3.8.3 Power-Save State

The digital GPIOs can be programmed to retain their output state during power-saving modes.

Digital GPIOs cannot be used to wake the chip. Only the dedicated WAKE_UP (A6) pin can be used to wake the chip.

If the RESET_N (B6) pin is asserted while the chip is in any power-save mode, the chip will reboot, the retained digital GPIO state will be lost, and the pads will reset to high impedance.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stress beyond absolute maximum ratings may cause permanent damage to the device. Operation is only guaranteed for recommended operating conditions. Operation of the device outside of recommended conditions may result in reduced lifetime and reliability problems, even if the absolute maximum ratings are not exceeded.

Parameter	Min	Max	Unit
VBAT_PWR	-0.3	3.6	V
VBAT_PWR_TX	-0.3	3.6	V
VBAT_AON	-0.3	3.6	V
VDDIO	-0.3	3.6	V
RESET_N/WAKE_UP	-0.3	3.6	V
RF_IN	-0.3	1.0	V

Table 13: Absolute maximum and minimum voltage ratings

4.2 ESD Immunity

Parameter			Min	Max	Unit
Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI / ESDA / JEDEC JS001	RF Input	-1,000	1,000	V
		All pins except RF Input	-2,000	2,000	V
	Charged device model (CDM), per JESD22-C101	All pins	-500	500	V

Table 14: ESD immunity specifications

4.3 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient temperature	-40	-	85	°C
Storage temperature	-40	-	125	°C
VBAT_PWR	3.0	3.3	3.6	V
VBAT_PWR_TX	3.0	3.3	3.6	V
VBAT_AON	3.0	3.3	3.6	V
VDDIO	2.25	3.3	3.6	V

Table 15: Recommended operating conditions

4.4 Power Consumption

4.4.1 Active Transmit Current Consumption

MCS Index	Current consumption (mA) per BW at V _{BAT}				Current consumption (mA) per BW at V _{BAT_TX}			
	100% duty cycle, T _A =25°C, V _{BAT} =V _{DDIO} =3.3 V							
	1 MHz	2 MHz	4 MHz	8 MHz	1 MHz	2 MHz	4 MHz	8 MHz
10	51	N/A	N/A	N/A	281	N/A	N/A	N/A
0	52	51	50	59	279	243	160	132
1	52	51	50	59	278	243	159	131
2	51	51	50	59	277	243	158	130
3	51	51	50	59	266	242	158	130
4	49	50	50	59	221	221	152	130
5	44	47	48	58	144	174	128	125
6	42	44	46	57	118	119	109	106
7	36	39	44	54	88	96	98	95
8	34	38	43	52	69	78	83	81
9	32	N/A	40	49	54	N/A	63	58

Table 16: Transmit current consumption for V_{BAT}, V_{BAT_TX} separated

4.4.2 Active Receive Current Consumption

MCS Index	$V_{BAT} + V_{BAT_TX} + V_{DDIO}$ Current consumption (mA) per BW			
	100% duty cycle, $T_A=25^\circ\text{C}$, $V_{BAT}=V_{DDIO}=3.3\text{ V}$, RX signal at -70dBm			
	1 MHz	2 MHz	4 MHz	8 MHz
0	18	19	23	31
Max	18 (MCS9)	20 (MCS8)	25 (MCS9)	34 (MCS9)

Table 17: Active receive current consumption

4.4.3 Listen Receive Current Consumption

$V_{BAT} + V_{BAT_TX} + V_{DDIO}$ Current consumption (mA) per BW			
$T_A=25^\circ\text{C}$, $V_{BAT}=V_{DDIO}=3.3\text{ V}$, Rx signal at -70dBm			
1 MHz	2 MHz	4 MHz	8 MHz
17	18	21	29

Table 18: Listen receive current consumption

4.4.4 Low Power Current Consumption

Power Mode	Current Consumption		
	$T_A=25^\circ\text{C}$, $V_{BAT}=V_{DDIO}=3.3\text{ V}$		
	$V_{BAT} + V_{BAT_TX}$	V_{DDIO}	Unit
Hibernate	<1	<1	μA
Deep Sleep	<2	<1	μA
Snooze	<20	<1	μA
USB snooze	<500	<1	μA

Table 19: Low power current consumption

4.4.5 Standby Current Consumption (using SDIO/SPI Host Interface)

Mode	Condition: $T_A=25^{\circ}\text{C}$, $V_{BAT}=V_{DDIO}=3.3\text{ V}$	$V_{BAT} + V_{BAT_TX}$	V_{DDIO}	Unit
DTIM3	2 MHz channel, RTC=RTC_XTAL, beacon=long	176	<1	μA
DTIM10	2 MHz channel, RTC=RTC_XTAL, beacon=long	68	<1	μA
DTIM40	2 MHz channel, RTC=RTC_XTAL, beacon=long	33	<1	μA
DTIM3	2 MHz channel, RTC=RTC_XTAL, beacon=short	126	<1	μA
DTIM10	2 MHz channel, RTC=RTC_XTAL, beacon=short	52	<1	μA
DTIM40	2 MHz channel, RTC=RTC_XTAL, beacon=short	29	<1	μA

Table 20: Standby current consumption

The DTIM (Delivery Traffic Indication Message) number (DTIM x) indicates how often a Wi-Fi HaLow station in power-saving Snooze mode wakes to receive traffic from the access point. It is expressed as a multiple of beacon intervals (multiples of 102.4 ms).

For example, DTIM1 indicates that the station will wake up every 102.4 ms, while DTIM40 configures the station to wake up every 4.1 seconds.

Configuring DTIM is a complex compromise between power consumption and latency. Increasing the DTIM will reduce the average power consumption, as the station spends a greater proportion of time in Snooze mode, which consumes significantly less power than in Listen mode. However, since the station is unable to receive traffic in Snooze mode, increasing DTIM also increases latency.

DTIM settings should be optimized appropriately according to the use case.

4.5 RF Specifications

4.5.1 Frequency Range

The MM8108 radio operates in the frequency range from 850 MHz to 950 MHz.

4.5.2 Receiver

4.5.2.1 Sensitivity

Sensitivities for 10% packet error rate, 256-byte packets. Conditions are VBAT=3.3 V, 25°C

MCS Index	Modulation Scheme	Coding Rate	PHY Rate (Mbps) per BW				Minimum Receive Sensitivity (dBm) per BW			
			1 MHz	2 MHz	4 MHz	8 MHz	1 MHz	2 MHz	4 MHz	8 MHz
10	BPSK	1/2 x 2	0.17	N/A	N/A	N/A	-108	N/A	N/A	N/A
0	BPSK	1/2	0.33	0.72	1.5	3.3	-107	-104	-102	-98
1	QPSK	1/2	0.67	1.4	3.0	6.5	-105	-102	-99	-96
2	QPSK	3/4	1.0	2.2	4.5	9.8	-102	-99	-97	-93
3	16-QAM	1/2	1.3	2.9	6.0	13	-99	-97	-94	-90
4	16-QAM	3/4	2.0	4.3	9.0	20	-96	-93	-90	-87
5	64-QAM	2/3	2.7	5.8	12	26	-92	-89	-86	-83
6	64-QAM	3/4	3.0	6.5	14	29	-91	-88	-85	-81
7	64-QAM	5/6	3.3	7.2	15	33	-89	-86	-83	-80
8	256-QAM	3/4	4.0	8.7	18	39	-85	-82	-79	-76
9	256-QAM	5/6	4.4	N/A	20	43	-83	N/A	-78	-74

Table 21: Rate and receiver sensitivity

4.5.2.2 Adjacent Channel Rejection

Adjacent channel rejection is measured by setting the requested signal's strength 3 dB above the rate-dependent sensitivity specified in 4.5.2.1 and increasing the power of the interfering signal until a 10% PER is achieved for a PSDU length of 256 bytes.

The power difference between the interfering and requested channel is the corresponding adjacent channel rejection.

MCS Index	Adjacent Channel Rejection (dB) per BW					Non-Adjacent Channel Rejection (dB) per BW				
	IEEE Spec	1 MHz	2 MHz	4 MHz	8 MHz	IEEE Spec	1 MHz	2 MHz	4 MHz	8 MHz
0	16	25	24	24	25	32	47	48	47	46
2	11	17	17	17	18	27	39	41	40	40
4	4	11	11	11	12	20	32	34	33	33
7	-2	1	1	11	2	14	23	24	24	23
8	-7	0	-1	-1	-2	9	18	21	20	19
9	-9	-1	N/A	-1	-1	7	17	N/A	18	17

Table 22: Adjacent channel rejection

4.5.2.3 Maximum Input Power

The following table specifies the maximum input level at RF_IN for a specified MCS and PER.

Condition	Max	Unit
MCS=0, PER<1%	0	dBm

Table 23: Maximum receiver input power

4.5.3 Transmitter

The following transmit power levels are for IEEE compliance for 802.11ah. They do not consider any backoffs needed for regional spectrum compliance (e.g., FCC, IC, TELEC). TX power in edge channels will be limited by the restricted band edge in the regulatory regions.

MCS Index	Power output (dBm) at the filter per BW $T_A=25^{\circ}\text{C}$, $V_{BAT}=V_{DDIO}=3.3\text{ V}$, IEEE-compliant with 1.5 dB SEM margin			
	1 MHz	2 MHz	4 MHz	8 MHz
10	25.5	N/A	N/A	N/A
0	25.5	25.0	23.0	22.5
1	25.5	25.0	23.0	22.5
2	25.5	25.0	23.0	22.0
3	25.5	25.0	23.0	22.0
4	24.5	24.5	22.5	22.0
5	22.0	23.5	21.5	21.5
6	22.5	21.5	21.0	20.5
7	19.0	20.0	20.0	20.0
8	17.5	18.0	19.0	19.0
9	16.0	N/A	17.0	16.5

Table 24: Mean TX output power

4.6 Digital IO Voltage Specifications

Parameters	Description	VDDIO	Min	Max	Unit
V_{IL_VDDIO}	Low input threshold for all GPIO and SDIO pins	3.3	-	1.2	V
V_{IH_VDDIO}	High input threshold for all GPIO and SDIO pins	3.3	1.7	-	V
V_{OL_VDDIO}	Low output voltage for all GPIO and SDIO pins, with an 8mA load	3.3	-	0.25	V
V_{OH_VDDIO}	High output voltage for all GPIO and SDIO pins, with an 8mA load	3.3	2.9	-	V

Table 25: Digital IO voltage specifications

5 Application Circuit

5.1 Schematic

Figure 12 shows a reference schematic for the MM8108. Each subcircuit is outlined in the sections below.

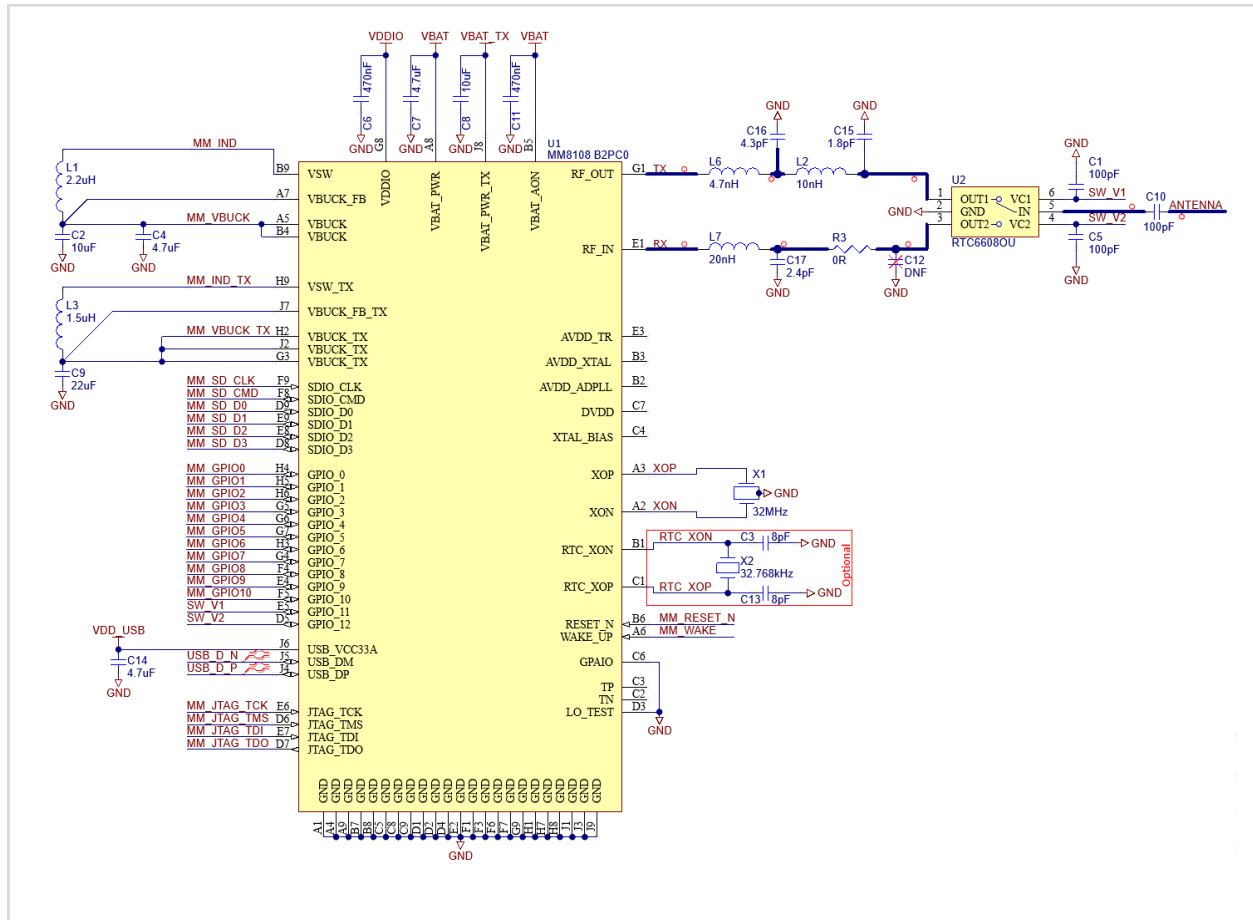


Figure 9: Reference schematic diagram

Bypass capacitor values should match those used in the reference design to ensure optimal device operation. Quality X5R or better decoupling capacitors are recommended to ensure stability over temperature and the device's lifetime.

The 2.2 uH and 1.5 uH buck inductors pass peak currents of 1 A, therefore, Isat and Itemp must be significantly greater than 1 A for these inductors. High-quality, low-DCR inductors are recommended for stability and reliability.

The reference design uses the following buck inductors:

- L1 (2.2 μ H): Murata DFE201612P-2R2M=P2
- L3 (1.5 μ H): Murata DFE201612P-2R2M=P2

Regulating VBAT and VBAT_TX is essential for performance. For a 500 mA load, VBAT should have less than 10 mV of ripple and 50 mV of load regulation.

5.2 Routing information

5.2.1 Buck Converter Routing

Spacing between the VSW (B9) pin and the inductor (L1) should be minimized, with the inductor and the capacitor of the LC filter placed close to one another. A low-impedance connection from the capacitor ground to the chip ground is required.

VBUCK and VBUCK_TX routing should be short and wide. VBUCK_FB and VBUCK_TX_FB routing should connect nearby to the load pins (VBUCK (A5 & B4) and VBUCK_TX (G3, H2 & J2) pins, respectively) and do not require wide routing, as these are high-impedance and for voltage sensing feedback only.

5.2.2 VBAT Routing

VBAT capacitors should be placed as close to the pins as possible with short and wide traces, not routing through vias between the capacitor and the VBAT_PWR (A8) pin. VBAT routing on the board should have low impedance, and more extended traces should be accounted for with increased capacitance at the pin to avoid VBAT sagging during load events. The capacitance illustrated in the application circuit is the minimal requirement for a well-regulated VBAT supply.

If an onboard LDO supplies VBAT, the feedback point should be at the VBAT_PWR_TX (J8) load pin or capacitor.

If a battery is used to supply VBAT directly, wide traces should be used to provide the best low-impedance path from the battery terminal to VBAT_PWR_TX (J8).

5.2.3 SPI/SDIO/JTAG Routing

Care should be taken to avoid coupling to the RF and buck sections. Impedance matching is unnecessary, but consistent trace widths and spacing are recommended to avoid signal integrity issues, with characteristic impedance not less than 50 Ω to avoid excess capacitive loading.

5.2.4 RF Routing

Impedance control to 50 Ω is required. Reference designs for TX filter and RX matching can be provided by Morse Micro on request, and complete reference designs with a TR switch can be included.

Care should be taken to isolate the RF section from all other parts of the circuit with low-impedance grounding and good spacing. For this purpose, a coplanar waveguide with ground is used in reference designs.

It is recommended to minimize impedance discontinuity by routing using components with pad sizes equal to or smaller than the 50 Ω trace. For the same reason, the inter-pad distance should be larger than the 50 Ω trace clearance to the coplanar ground.



Figure 10: Trace diagram

Component placement should target the shortest overall trace length to minimize losses.

5.3 RF Section

5.3.1 Transmitter

The output is purposefully mismatched away from $50\ \Omega$ to optimize power consumption and output power. To meet worldwide regulatory requirements, an external harmonic filter, as shown below, must be included in the design. This filter must be copied precisely, as modification negatively affects efficiency and output power.

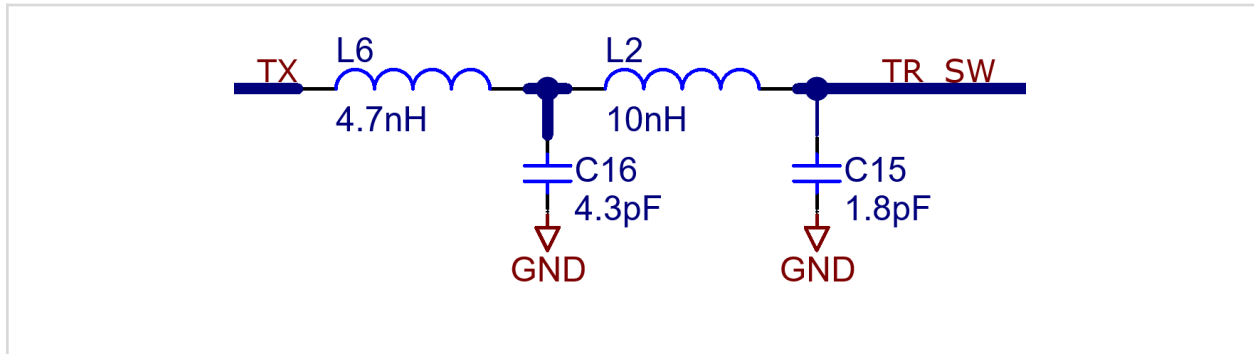


Figure 11: Transmission filter diagram

The layout recommendations from Figure 13 apply.

The reference design uses the following components:

- L6 (4.7 nH): Murata LQP03HQ4N7H02D
- C16 (4.3 pF): Murata GRM0335C1H4R3WA01D
- L2 (10 nH): Murata LQP03HQ10NH02D
- C15 (1.8 pF): Murata GRM0335C1H1R8WA01D

5.3.2 Transmit/Receive RF Switch

The reference design uses $50\ \Omega$ TR switches with low insertion loss and high isolation. Note the requirement for DC-blocking capacitors on the TR switch's RF ports.

5.3.3 Receiver Matching

The receiver is matched to ensure an optimal balance between noise tolerance and signal sensitivity over the usable bandwidth. The reference circuit will result in optimal performance.

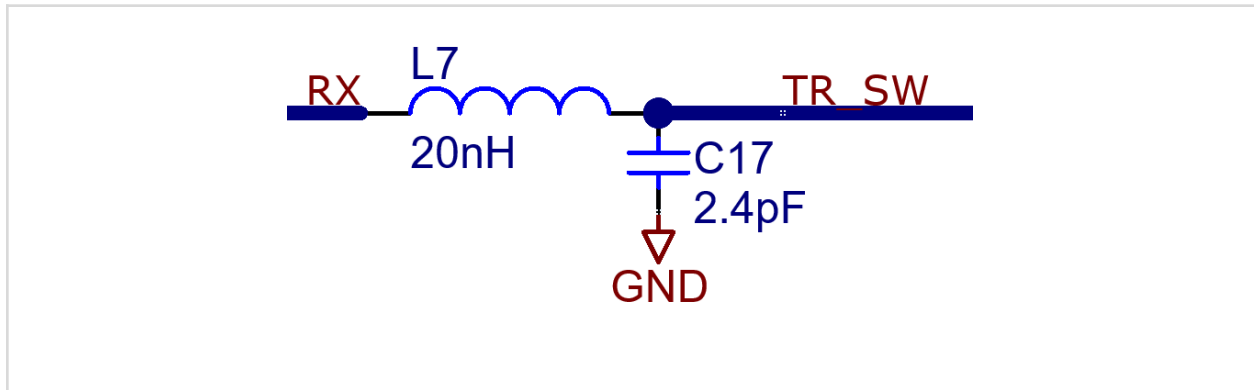


Figure 12: Receiver matching diagram

The reference design uses the following components:

- L7 (20 nH): Murata LQP03HQ20NH02D
- C17 (2.4 pF): Johanson 250R05L2R4BV4T

5.3.4 Antenna/Interstage Matching

Interstage matching may be required to minimize losses depending on the antenna, TR switch, and external active components used. Standard techniques are recommended to match each port to an intermediate impedance of $50\ \Omega$. Matching to an intermediate of $50\ \Omega$ results in a more robust design since each component can be individually matched to $50\ \Omega$ without considering inter-device effects.

6 Package Information

6.1 Package Dimensions

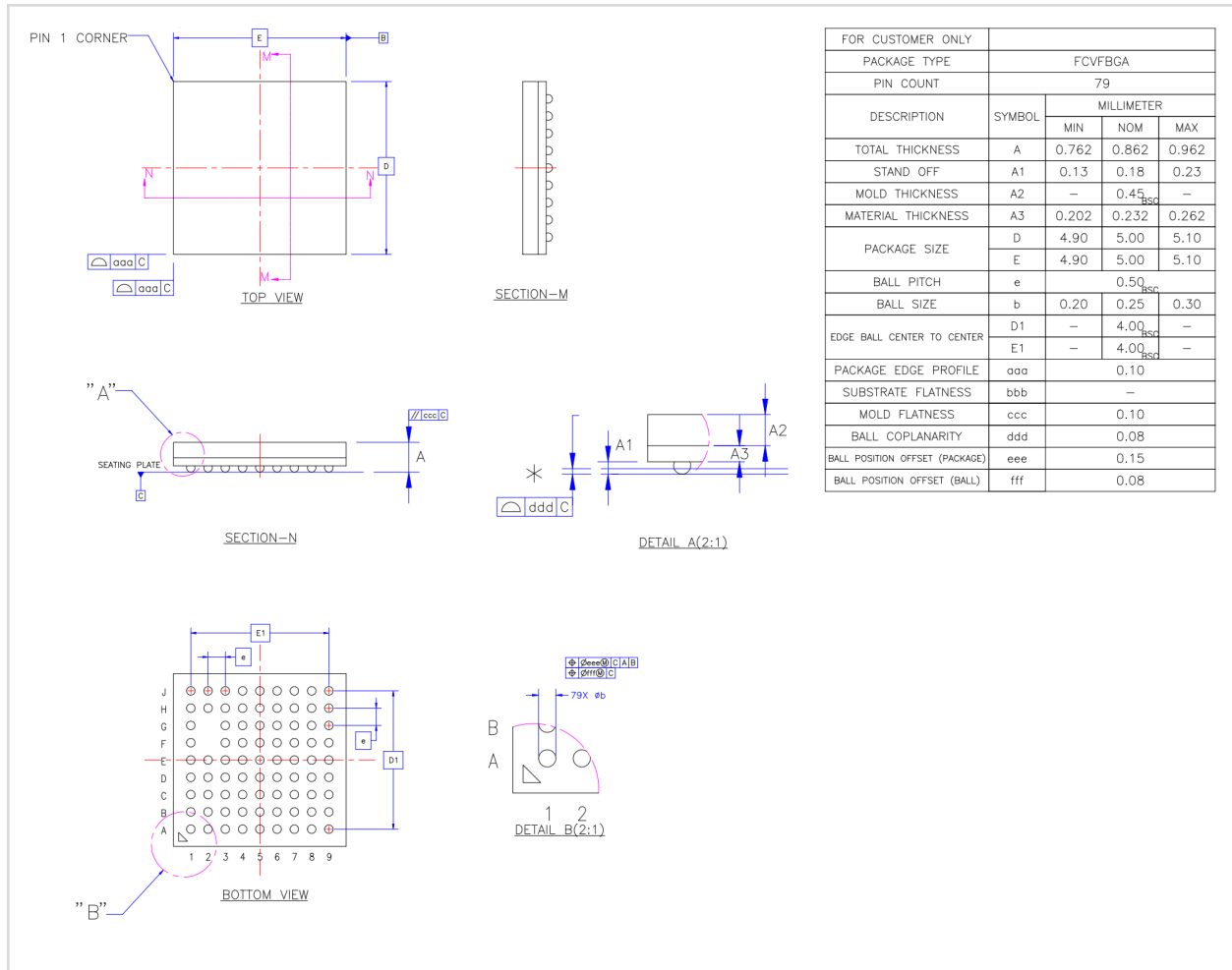


Figure 13: Package dimensions

6.2 IC Markings

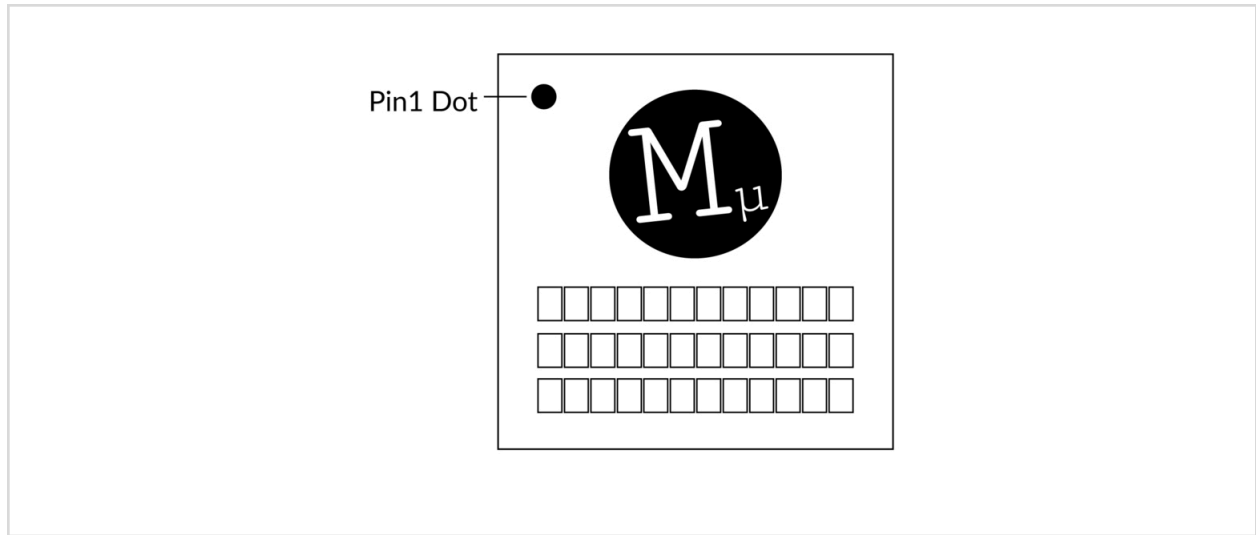


Figure 14: IC markings diagram

Line	Marking	Example	Description
1	MMXXXXDS	MM8108IB	Device number (XXXX); Optional: Custom marketing letter; Temperature grade (D); Package type (S);
2	TA22 YYWW	TA22 2401	Fab/Assembly codes; 2 digits for Silicon revision (Major, Minor - Internal Only); date code YYWW;
3	XXXXXXXX	341N001	Assembly lot number

Table 26: IC markings overview

Marking	Purpose	Example	Description
M	Major silicon revision	0..9	Designated by a single number from 0 to 9
N	Minor silicon revision	0..9	Designated by a single number from 0 to 9
D	Temperature grade	I/C	I = -40°C to 85°C; C = 0°C to 70°C
S	Package Type code	Q/B	Q: QFN; B: FCBGA/BGA

Table 27: IC markings details

6.3 Package Thermal Properties

Ball count	Size	Power (W)	T _A (°C)	Θ _{JA} (°C/W)	Θ _{JC} (°C/W)	Θ _{JB} (°C/W)	Ψ _{JB} (°C/W)	Ψ _{JT} (°C/W)
79	FCCSP 5x5	0.5	25	31.794	6.882	7.18	1.092	1.368
			55	27.084	6.882	7.17	1.164	1.366

Table 28: Package thermal properties overview

T_A: Ambient temperature

Θ_{JA}: Thermal resistance junction-to-ambient

Θ_{JC}: Thermal resistance junction-to-case

Θ_{JB}: Thermal resistance junction-to-board

Ψ_{JB}: Thermal characterization parameter junction-to-board

Ψ_{JT}: Thermal characterization parameter junction-to-top (of package)

Notes:

- JESD51 test standards used
- PCB is JEDEC 2S2P test board
- Board level solder is SAC405 (thickness = 50 μm)
- The maximum junction temperature must be controlled to ≤ 125 °C

7 PCB Land Pattern

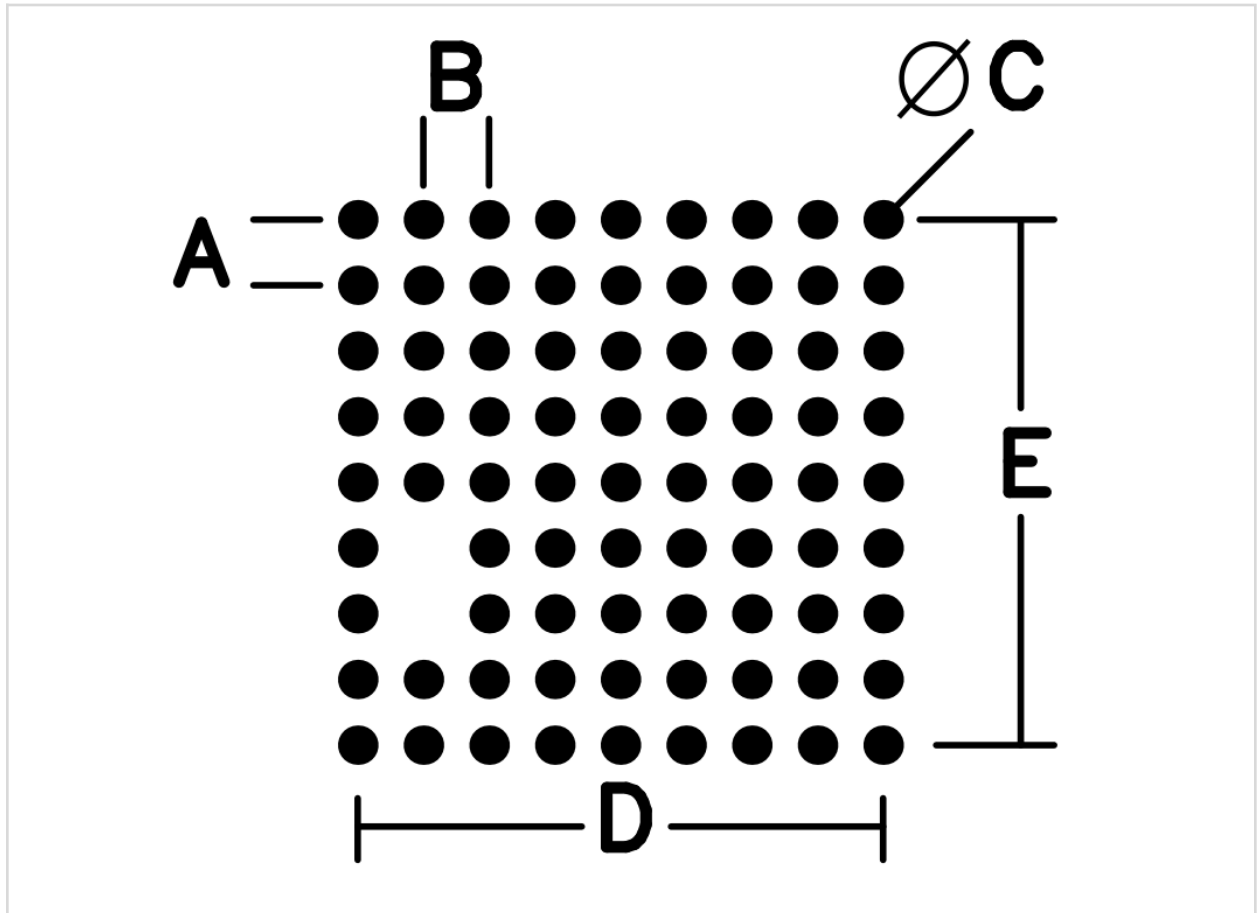


Figure 15: PCB land pattern

Key	Dimension (mm)
A	0.5
B	0.5
C	0.3
D	4.0
E	4.0

Table 29: PCB land pattern dimensions

8 Solder Stencil Pattern

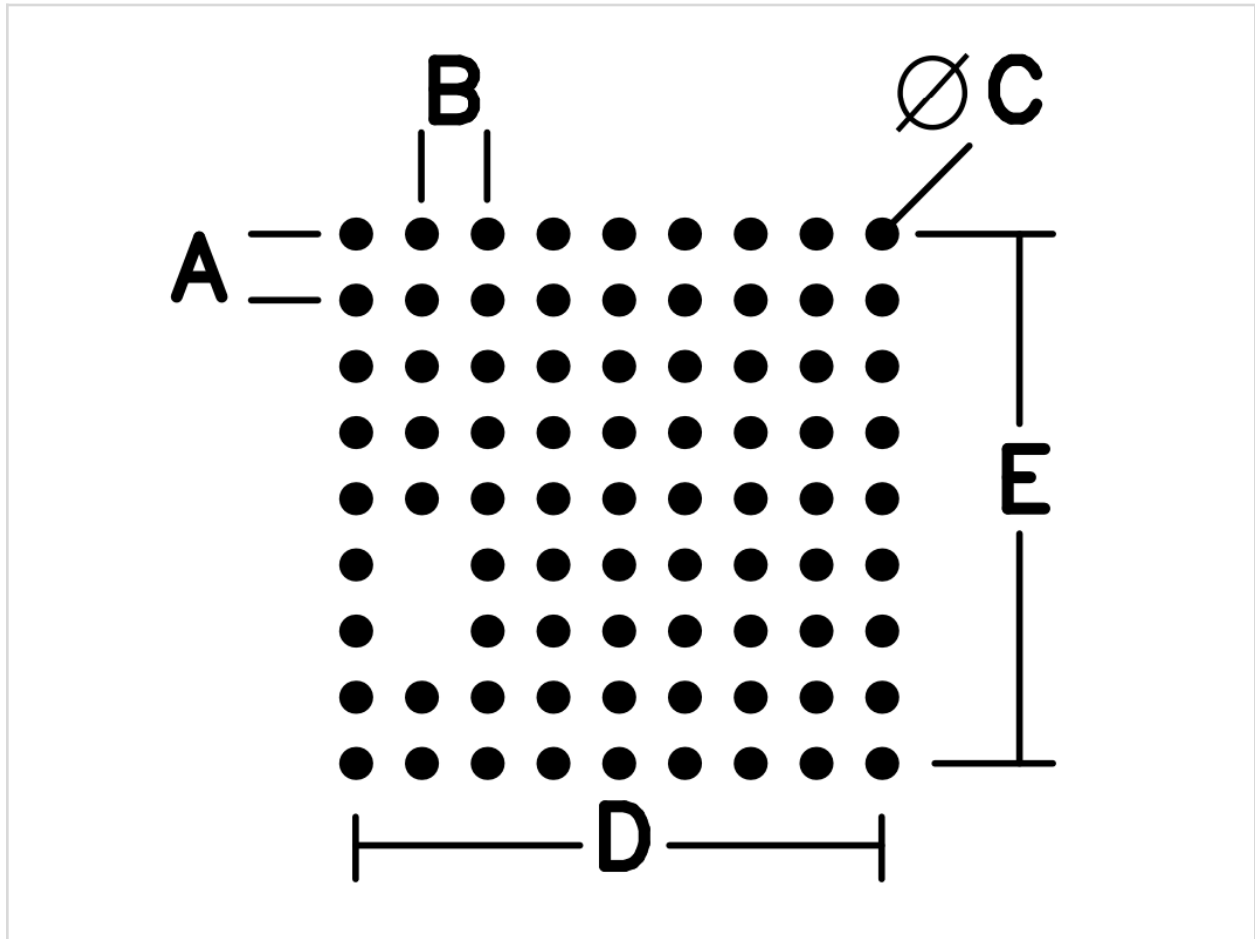


Figure 16: Solder stencil pattern

Key	Dimension (mm)
A	0.5
B	0.5
C	0.275
D	4.0
E	4.0

Table 30: Solder stencil pattern dimensions

9 Recommended Soldering Profile

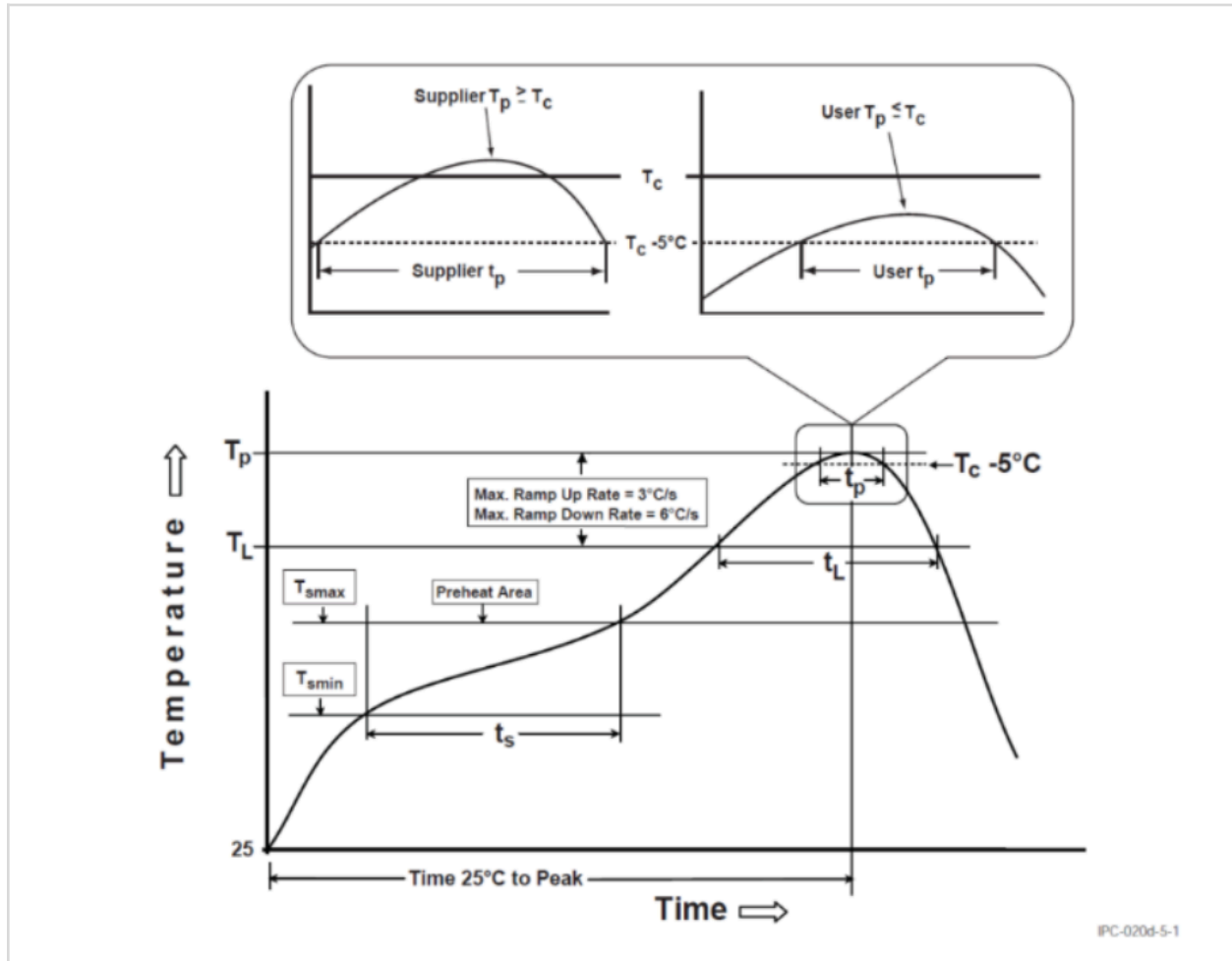


Figure 17: Soldering profile

Soldering profile feature	Specification
Classification temperature (T_C)	260 °C
Min soak temperature (T_{smin})	150 °C
Max soak temperature (T_{smax})	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Liquidus temperature (T_L)	217 °C
Maximum ramp-up rate (T_L to T_P)	3 °C per second
Time (t_L) maintained above T_L	60-150 seconds
Peak package body temperature (T_P)	For users, T_P must not exceed the T_C For suppliers, T_P must equal or exceed T_C
Time (t_p) within 5 °C of the specified classification temperature (T_C)	For users, a maximum of 30 seconds For suppliers, a minimum of 30 seconds
Maximum ramp-down rate (T_P to T_L)	6 °C per second
Maximum time 25 °C to peak temperature (T_P)	8 minutes

Table 31: Soldering profile details

Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.

In other words, if T_C is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user:

- For a supplier, the peak temperature must be at least 260 °C, and the time above 255 °C must be at least 30 seconds.
- For a user, the peak temperature must not exceed 260 °C, and the time above 255 °C must not exceed 30 seconds.

All temperatures refer to the center of the package, measured on the package body surface facing up during assembly reflow (live-bug). If parts are reflowed in a different orientation than the normal live-bug assembly reflow orientation (dead-bug), the T_P must be within +/- 2 °C of the live-bug T_P and still meet the T_C requirements; otherwise, the profile shall be adjusted to achieve the latter. To accurately measure peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and within the parameters above.

10 Packaging and Labeling

10.1 Tray Specifications

Term	Definition
Product	MM8108
Number of units	490
Tray size	322.6 mm x 135.9 mm
Vacuum seal	Yes
Dry bake	125 °C / 24 hours (ML3)
Pin 1 indicator	Marked on the chip

Table 32: Tray specifications

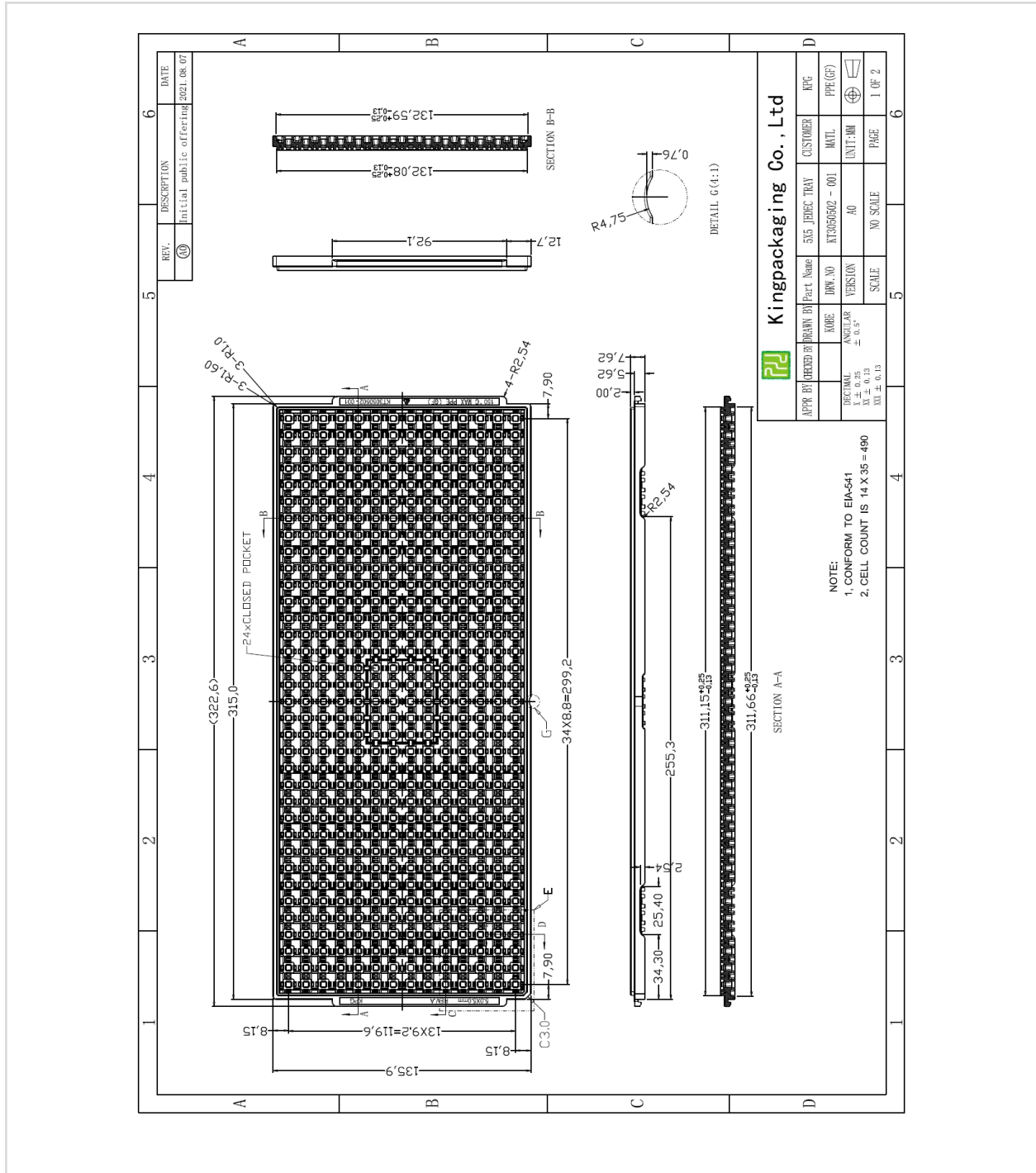


Figure 18: Tray specifications

11 Handling and Storage

The MM8108 IC is a moisture-sensitive device rated at Moisture Sensitive Level 3 (MSL3) per IPC/JEDEC J-STD-20.

After opening the moisture-sealed storage bag, ICs that will be subjected to reflow solder or other high-temperature processes must be:

1. Mounted to a circuit board within 168 hours at factory conditions ($\leq 30^{\circ}\text{C}$ and $< 60\% \text{ RH}$)

OR

2. Continuously stored per IPC/JEDEC J-STD-033

ICs exposed to moisture and environmental conditions exceeding packaging and storage conditions must be baked before mounting according to IPC/JEDEC J-STD-033. Failure to meet packaging and storage conditions will result in irreparable damage to chips during solder reflow.

12 Part Number and Ordering Information

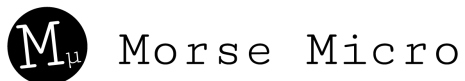
Part Number	Packing Type	MOQ and Order Multiples	Package	Description	Operating Ambient Temperature
MM8108IB-T	Tray	490	BGA 5 mm x 5 mm	Multi-region Wi-Fi HaLow / IEEE 802.11ah Sub-1 GHz SoC with USB Interface and Integrated Power and Low Noise Amplifiers	-40 °C to 85 °C
MM8108IB-TR	Tape & Reel	3000			

Table 33: Part number and ordering information

13 Revision History

Release Number	Release Date	Release Notes
Version 4	18 Sep 2025	Updated formatting Update pin descriptions Updated power management Updated timing graphs Updated electrical specifications Updated RF specifications Added digital IO specifications Added PCB land solder stencil patterns
DS102	8 Jan 2025	General update
DS101	4 Nov 2024	Add packaging and handling information Add soldering information Add labeling information
DS100	1 Nov 2024	Initial release

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