Morse Micro

MM6108 SoC
Data Sheet

Wi-Fi HaLow / IEEE 802.11ah
Sub-1 GHz 1/2/4/8 MHz Bandwidth
MAC/PHY/Radio SoC

Table of Contents

1 Product Overview

1.1 Introduction

Wi-Fi HaLow (pronounced HEYlow) is the first global Wi-Fi standard (IEEE 802.11ah) tailored to meet the Internet of Things (IoT) needs. It's an open standard wireless network technology operating in the sub-1 GHz license-exempt RF bands (850-950 MHz range), so it doesn't incur ongoing monthly costs like cellular/mobile network connections. By operating in the sub-GHz range, this ultra-low-power wireless protocol can connect more IoT devices at much longer distances and with much lower power than traditional Wi-Fi.

Morse Micro, the world's leading Wi-Fi HaLow (802.11ah) solutions provider, offers several Wi-Fi HaLow connectivity solutions. The MM6108 SoC is a single-chip solution that includes Radio, PHY, and MAC functions compliant with the IEEE 802.11ah standard and supports data rates up to 32.5 Mbps. The radio in the MM6108 supports programmable operation between 850 MHz and 950 MHz.

The MM6108 has been designed for a simplified Wi-Fi HaLow connection to an external host.

The RF interface for the MM6108 includes the option to use either the on-chip amplification for typical low-power, low-cost devices or in conjunction with an external PCB mounted power amplifier for ultra-long-reach applications.

The RF receiver features a high linearity LNA, making external filters unnecessary in many applications.

MM6108 supports security features required for Wi-Fi HaLow product certifications.

A combination of features in the MM6108 supports battery-operated applications. The IEEE 802.11ah standard provides extended sleep times of battery-operated Stations (STAs or client devices), with longer durations than other prior IEEE 802.11a/b/g/n/ac generations. It also allows longer extended maximum idle times for clients to conserve energy without being removed from the Access Point's list of authenticated devices.

1.2 Features

- Single-stream max data rate of 32.5 Mbps (MCS=7, 64-QAM, 8 MHz channel, 4µs GI)
- Radio supporting worldwide Sub-1 GHz frequency bands
    - Frequency range: 850-950 MHz
    - Channel bandwidth options of 1/2/4/8 MHz
    - Max output power: 8 dBm
- 802.11ah OFDM PHY
    - BPSK & QPSK, 16-QAM & 64-QAM Modulation
    - Automatic frequency & gain control
    - Packet detect & channel equalization
    - Forward Error Correction (FEC) coding & decoding
    - Supports Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
    - Supports 1 MHz duplicate mode
    - Supports optional Traveling Pilots and Short Guard Intervals
- 802.11ah MAC supporting WFA HaLow certification
    - Support for STA and AP roles
    - Listen-Before-Talk (LBT) access with energy detect
    - 802.11 power save
    - 802.11 fragmentation and defragmentation
    - Packet aggregation
    - Power-Saving Target Wake Time (TWT) support for long battery life
    - Restricted Access Window (RAW)
    - Automatic and manual MCS rate selection
- SDIO 2.0 compliant slave interface
    - SDIO 2.0 Default Speed (DS) at 25 MHz
    - SDIO 2.0 High Speed (HS) at 50 MHz
    - Support for both 1-bit and 4-bit data mode
    - Support for SPI mode operation
- Power Management Unit (PMU) for various modes of operation
    - Power-down (interrupt-driven wake)
    - Hibernate mode (internal/external wake)
    - Active Receive / Transmit mode
    - Integrated DC-DC converter supporting a voltage supply from 3.0V to 3.6V
- RF Interface
    - On-chip 8dBm output power, with option to use external PA or FEM
    - Option to use an external LNA or FEM
- Wide spectrum of security features
    - AES encryption engine
    - Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
    - WPA3, including protected management frames (PMF)
    - Opportunistic Wireless Encryption (OWE)

1.3 Applications

For Internet of Things (IoT) and Machine-to-Machine (M2M) applications such as:

- Surveillance Cameras and Sensors
- Cloud Connectivity
- Low-power Sensor Networks
- Building Automation Systems (BAS)
- Asset Tracking and Management
- Machine Performance Monitors & Sensors
- Building Access Control & Security
- Drone Video and Navigation Communications
- Connected Toys and Games
- Rural Internet Access
- Agricultural and Farm Networks
- Utility Smart Meter and Intelligent Grid
- Proximity Sensors
- Industrial Automation Controls
- Smart Home Automation
- EV Car Chargers
- Appliances
- Construction Site Connectivity
- Smart Signs and Kiosks
- Retail Point-of-Sale Terminals
- Vehicle-to-Vehicle or Vehicle-to-Infrastructure Communications
- IP Sensor Networks
- Biometric IDs and Keypads
- Warehouse Connectivity
- Intelligent Lighting Controls
- BT/ZigBee(™)/Z-Wave(™) to Wi-Fi HaLow Gateways
- Wi-Fi to Wi-Fi HaLow Bridges
- Wi-Fi HaLow Client Adapters/Dongles
- Smart City Networks

2 Pin Descriptions

The MM6108 device has 48 pins, which are described in this section. The following illustration shows the top view of the MM6108 pin Diagram.

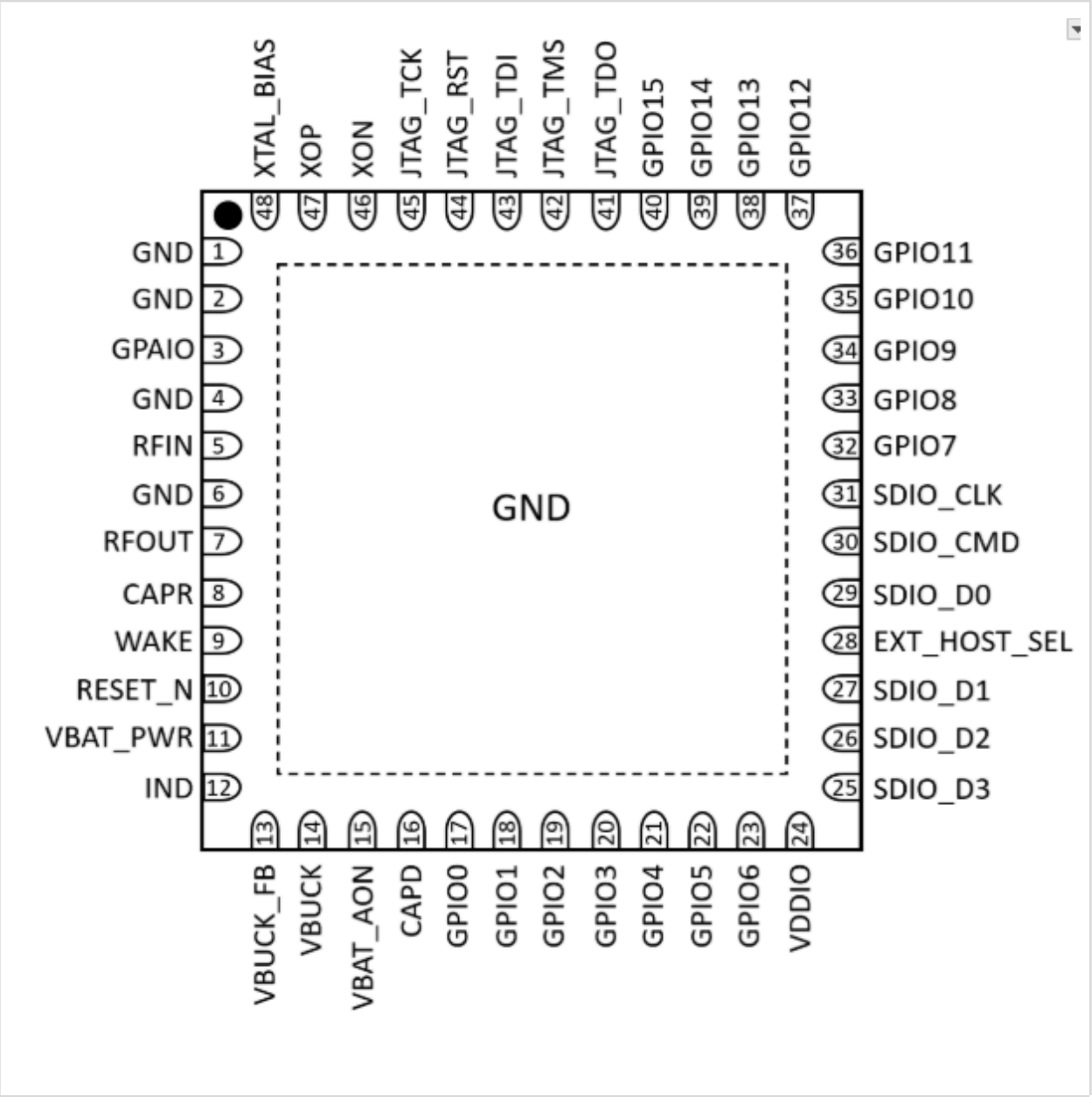


Figure 1: Pin diagram

Pin	Pin Name	Type	Description
1	GND	Ground	Ground
2	GND	Ground	Ground
3	GPAIO	Analog	Analog test pin
4	GND	Ground	Ground
5	RFIN	RF	RF input
6	GND	Ground	Ground
7	RFOUT	RF	RF output
8	CAPR	Power	Bypass capacitor connection for RF supply
9	WAKE[4]	Input	WAKE from sleep input
10	RESET_N[4]	Input	Asynchronous chip reset (active low)
11	VBAT_PWR	Power	IC Power Supply
12	IND	Analog	Inductor connection for integrated power management
13	VBUCK_FB	Power	Connection for integrated power management
14	VBUCK	Power	Connection for integrated power management
15	VBAT_AON	Power	IC Power Supply (VBAT_AON and VBAT_PWR must be connected to the same source)
16	CAPD	Power	Bypass capacitor connection for digital supply
17	BUSY[5]	Digital I/O	Wi-Fi Busy
18	GPIO1[5]	Digital I/O	GPIO
19	GPIO2[5]	Digital I/O	GPIO
20	GPIO3[5]	Digital I/O	GPIO
21	GPIO4[5]	Digital I/O	GPIO
22	GPIO5[5]	Digital I/O	GPIO
23	GPIO6[5]	Digital I/O	GPIO
24	VDDIO	Power	VDD supply for digital IO
25	SDIO_D3[3][5]	Digital I/O	SDIO Data 3
26	SDIO_D2[3][5]	Digital I/O	SDIO Data 2
27	SDIO_D1[3][5]	Digital I/O	SDIO Data 1
28	EXT_HOST_SEL[5]	Digital I/O	External Host Select
29	SDIO_D0[3][5]	Digital I/O	SDIO Data 0
30	SDIO_CMD[3][5]	Digital I/O	SDIO Command
31	SDIO_CLK[5]	Digital I/O	SDIO Clock
32	GPIO7[2][5]	Digital I/O	GPIO
33	GPIO8[2][5]	Digital I/O	GPIO
34	GPIO9[2][5]	Digital I/O	GPIO
35	GPIO10[2][5]	Digital I/O	GPIO
36	GPIO11[2][5]	Digital I/O	GPIO/ RF FEM CTRL

Pin	Pin Name	Type	Description
37	GPIO12[2][5]	Digital I/O	GPIO/ RF FEM CTRL
38	GPIO13[2][5]	Digital I/O	GPIO/ RF FEM CTRL
39	GPIO14[2][5]	Digital I/O	GPIO/ RF FEM CTRL
40	GPIO15[2][5]	Digital I/O	GPIO/ RF FEM CTRL
41	JTAG_TDO[1]	Digital I/O	JTAG Data Out
42	JTAG_TMS[1]	Digital I/O	JTAG Mode Select
43	JTAG_TDI[1]	Digital I/O	JTAG Data In
44	JTAG_TRST[1]	Digital I/O	JTAG Reset
45	JTAG_TCK[1]	Digital I/O	JTAG Clock
46	XON	Analog	32 MHz crystal component connection
47	XOP	Analog	32 MHz crystal component connection
48	XTAL_BIAS	Analog	Crystal Bias
-	GND	Ground	Exposed ground pad - must connect to PCB ground

Table 1: Pin description

[1] JTAG pins should be tied to GND via a 10k pull down resistor
[2] All unused GPIO should be tied to GND via a 10k pull down resistor
[3] All SDIO bus pins should be pulled up with a 10k-100k resistor as per the SDIO standard
[4] Supplied from VBAT domain. The VDDIO domain drives other pins.
[5] See Section 4.1 for the GPIO Alternate functions

3 Functional Description

The following sections describe the functions of the MM6108 SoC.

3.1 Functional Block Diagram

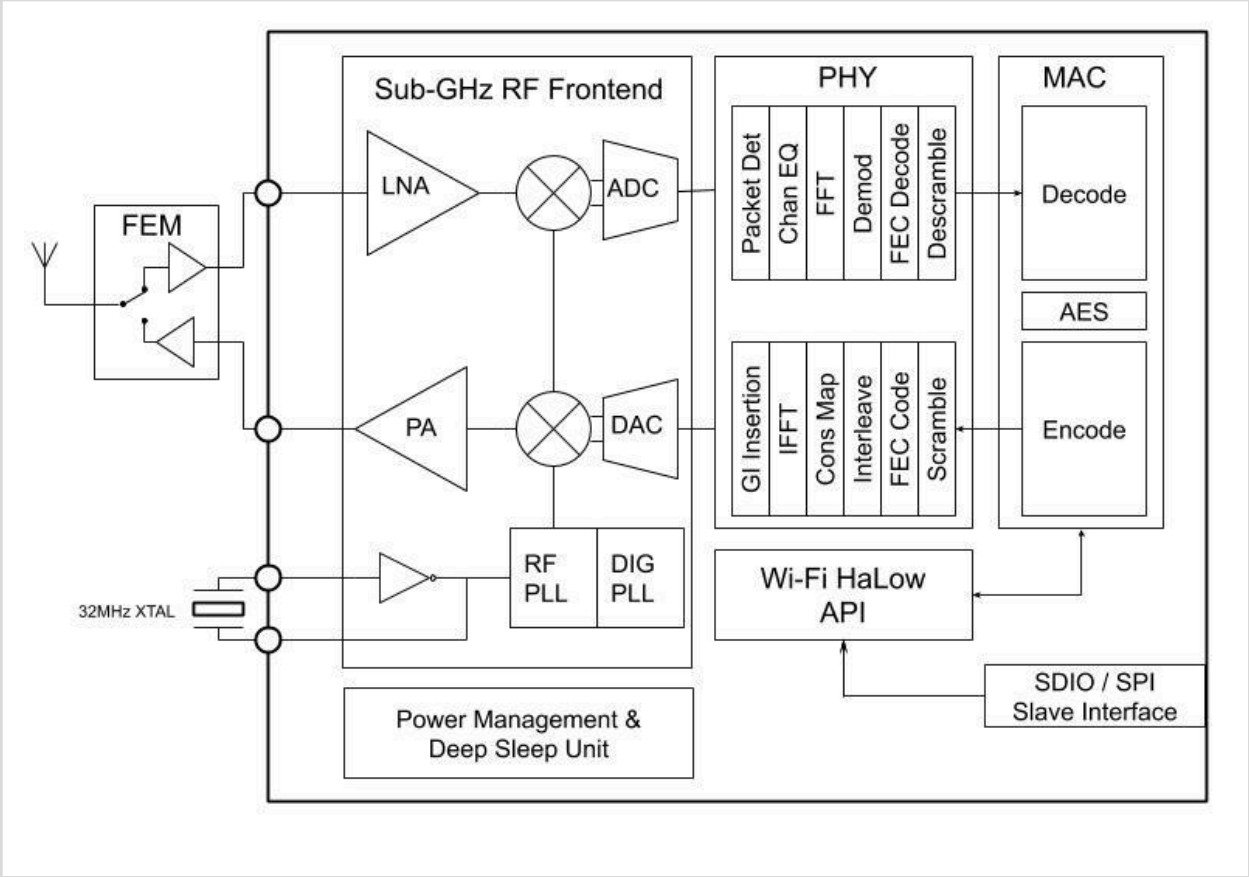


Figure 2: Functional Block Diagram

3.2 Clocks

The MM6108 uses a 32 MHz crystal component to derive all the clocks used in the system. A Pierce oscillator circuit is used as shown below:

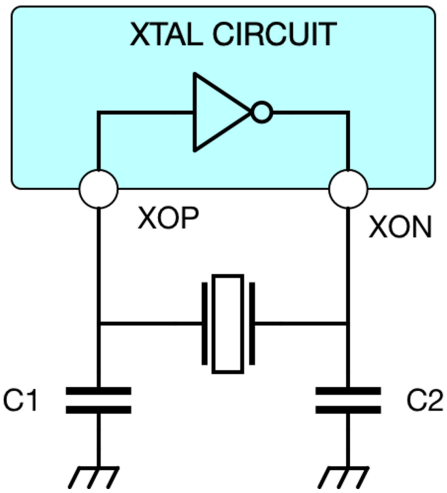


Figure 3: Crystal circuit

The crystal should be connected between pins XOP & XON. Load capacitors C1 and C2 should be high-accuracy NP0 dielectric. The total capacitance on XOP and XON nodes should be twice that of the load capacitance specified by the crystal component (CL):

C1 = C2 = 2 x CL

To adhere to 802.11ah standards for frequency offset and achieve specified sensitivity, the crystal component should conform to the following specifications:

Parameter	Min	Max	Units
Frequency tolerance	-20	+20	ppm
ESR	10	50	ohm

Table 2: RF crystal specification

3.3 Power Management

All power is derived from a 3.0V to 3.6V supply on pin VBAT_PWR and VBAT_AON. To avoid damage to the device, ensure that VDDIO does not exceed VBAT.

An internal buck converter requires a 10uH inductor between pins IND and VBUCK_FB and ceramic decoupling capacitors as shown below.

There are three internal power supplies: RF, Analog, and Digital. Internal circuits regulate these and require ceramic decoupling capacitors on the PCB at CAPR, CAPD, and VBAT_AON as shown below.

For regular boot operation, ensure that the JTAG_TRST pin is held in reset by pulling it to ground with a 10kOhm resistor.

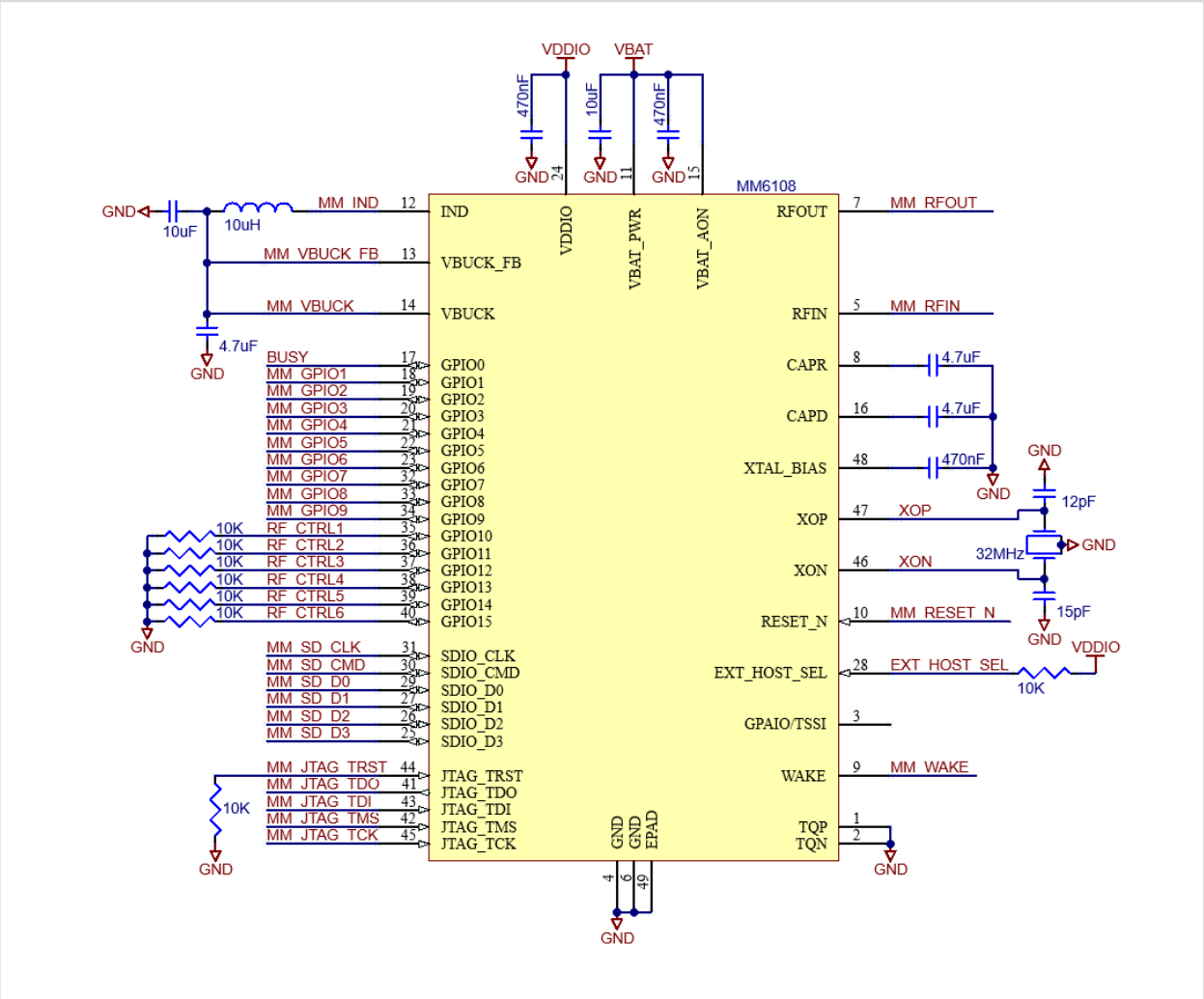


Figure 4: Reference schematic diagram

4 Digital Interfaces

4.1 SDIO Device

A host interface is available via SDIO 2.0, operating at 3.3V at either default or high speed. To expose the SDIO interface pins, pin 28 EXT_HOST_SEL must be pulled up to VDDIO, indicating the presence of an external host.

4.1.1 Pins

Pin	Name	SDIO 4-bit mode	SDIO 1-bit mode
25	D3	Data pin 3	Unused
26	D2	Data pin 2	Unused
27	D1	Data pin 1	IRQ
28	EXT_HOST_SEL	SDIO/SPI/QSPI interface enable strap (tie high)	
29	D0	Data pin 0	
30	CMD	Command pin	
31	CLK	Clock pin (input)	

Table 3: SDIO pin description

Note: All SDIO lines should be pulled up to VDDIO with 10 kΩ to 100 kΩ resistors as per the SDIO 2.0 Specification. SDIO_CLK and unused pins should also be pulled up to achieve ideal sleep/snooze currents if not driven by a host processor.

4.1.2 Functions

Internally, the SDIO will present two functions (in addition to the mandatory function 0) to access the chip. Functions 1 and 2 only differ in the maximum transfer size they support. Function 1 can perform transactions up to 8 bytes at a time, while function 2 supports up to 512 bytes at a time, making it better suited to bulk data transfers.

4.1.3 Bus Timing

The SDIO interface supports a clock rate up to 50 MHz.

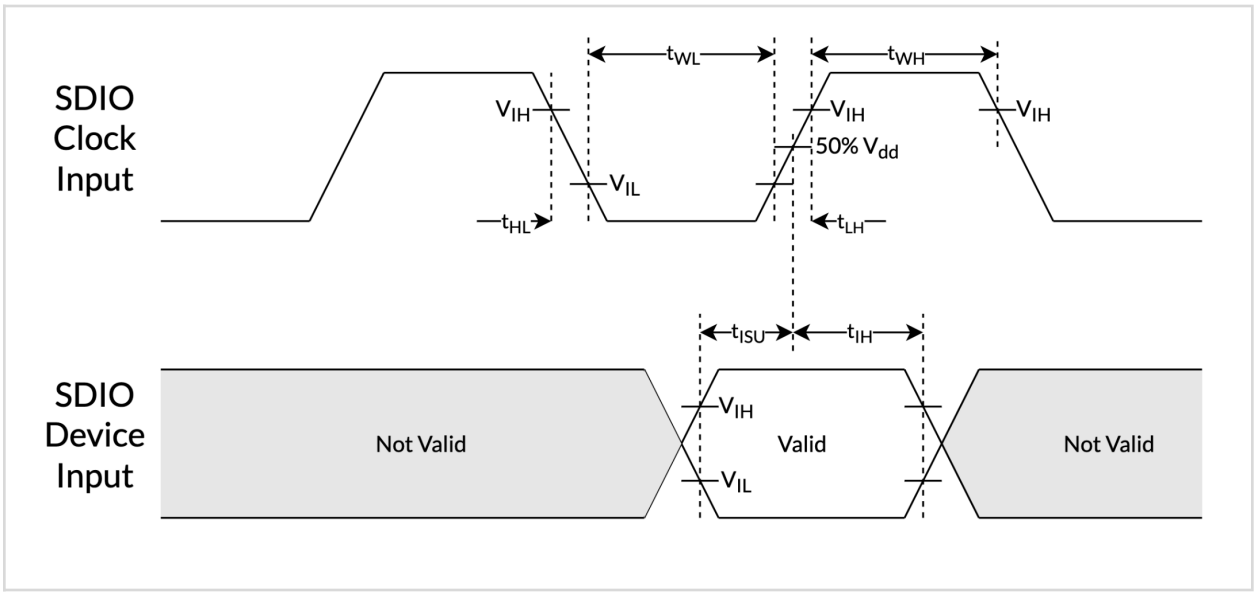


Figure 5: SDIO bus device input timing diagram

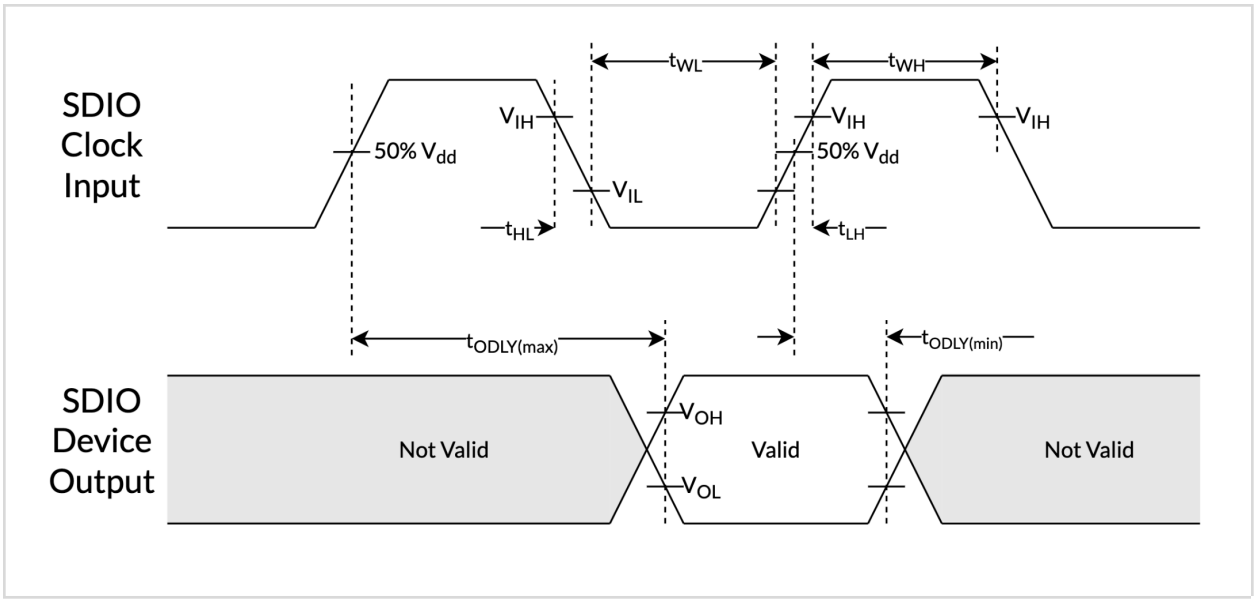


Figure 6: SDIO bus device output timing diagram

Parameter	Min	Max	Units
Clock frequency	0	50	MHz
Clock low time (t_{WL})	7		ns
Clock high time(t_{WH})	7		ns
Clock rise time (t_{LH})		3	ns
Clock fall time (t_{HL})		3	ns
Input setup time (t_{ISU})	6		ns
Input hold time (t_{IH})	2		ns
Output delay ($t_{ODLY(max)}$)		14	ns
Output hold time ($t_{ODLY(min)}$)	2.5		ns
Total system capacitance for each line		40	pF

Table 4: SDIO Bus Timing

4.2 SPI Device

The SPI interface uses the physical unidirectional pin layout defined below, and it communicates using the modified SDIO protocol.

4.2.1 Pins

Pin	Name	SPI mode function
25	CS	Chip select (active low)
26	NC	Not connected/unused (tie to VDDIO)
27	INT	Interrupt pin
28	EXT_HOST_SEL	SDIO/SPI/QSPI interface enable strap (tie to VDDIO)
29	MISO	Master data in/slave data out
30	MOSI	Master data out/slave data in
31	CLK	Clock pin (input)

Table 5: SPI pin description

4.2.2 Initialization in SPI mode

After powering on, the host interface can be either SDIO or SPI. To switch to SPI mode, the host must send a CMD0 while holding CS low (asserted).

For further details on the protocol, see SD Specification Part E1, “SDIO Simplified Specification,” version 2.00.

4.2.3 SPI Bus Timing

The SPI clock rate supports up to 50 MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are input and output timing in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per the SDIO high-speed mode. After being initialized, it may be configured to behave like CPHA=0 (drive output on the negative edge, sample on the positive edge).

4.3 GPIO

There are 16 GPIO pins. These will be high-impedance at reset and during power save modes. These pins should be pulled up/down or driven to ensure the lowest sleep currents.

4.4 Sleep/Wake Sequencing

4.4.1 Host wakes MM6108 from sleep

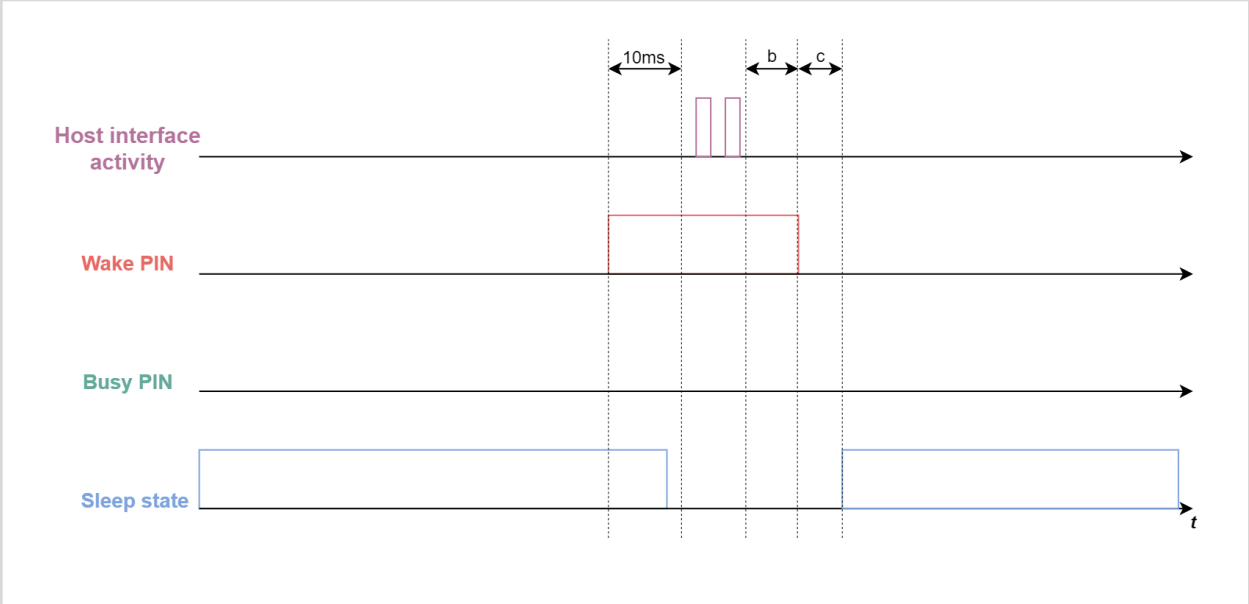


Figure 7: Host-initiated wake sequence diagram

1. The driver raises the wake pin and waits for a static period of 10 ms before initializing the shared communication bus and initiating host interface activity. On MM6108, this period is typically 10 ms.
2. After completing communication, the driver will wait a static period, b, before lowering the wake pin (assuming no further communication has occurred). Depending on the nature of the communication (802.11 data vs. commands), this period can range from 5 to 90ms.
3. After the wake pin has fallen, the MM6108 will wait for a period, c, before initiating hardware sleep. This dynamic period will differ depending on the power-saving protocol and other chip-specific factors.

4.4.2 MM6108 wakes host from sleep (with host interface disabled)

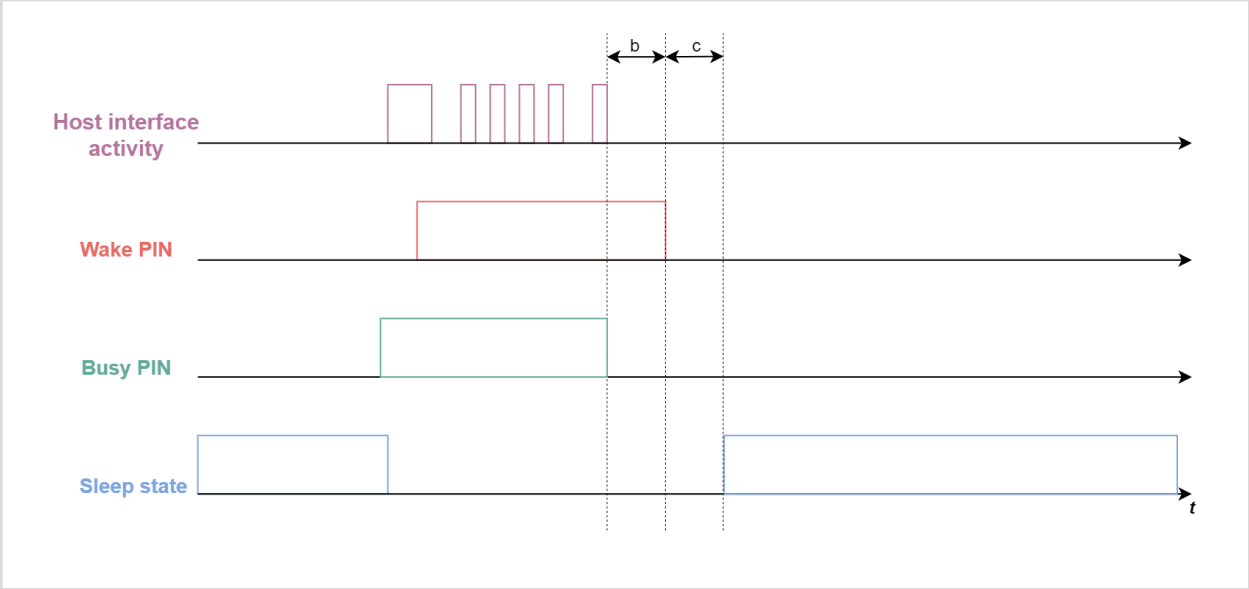


Figure 8: Module-initiated wake sequence with host interface disabled diagram

1. The MM6108 wakes from sleep and realizes it needs to pass traffic or an event to the host. It begins by asserting the busy pin.
2. The busy pin will fire an interrupt on the host, after which the host will immediately:
    a. Raise the Wake PIN.
    b. Wait a static period, 10ms
    c. Initializes / enables the shared host interface.
3. After asserting the busy pin, the MM6108 will initiate host interface communication immediately. It does not wait until the host 'enables' the shared host interface. This is okay, as the bus transaction will be waiting for the host, and an interrupt should fire as soon as the host enables bus interrupts.
4. The busy pin will drop immediately once the MM6108 no longer needs to converse with the host. The host will wait a static period, b, before dropping the wake pin.
5. After the wake pin has fallen, the MM6108 will wait for a period, c, before initiating hardware sleep.

4.4.3 MM6108 initiates communication with the host (host interface enabled)

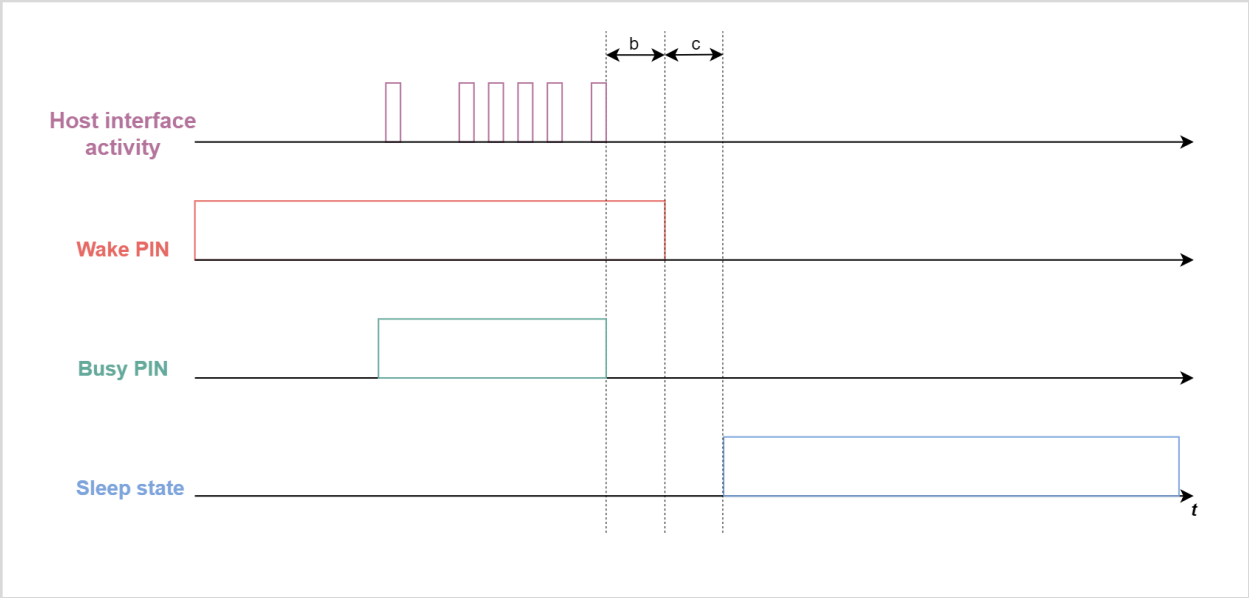


Figure 9: Module-initiated wake sequence with host interface enabled diagram

1. The MM6108 was previously woken by the host for communication.
2. Sometime after wake and host->MM6108 communication, the MM6108 realizes it needs to send data back to the host (MM6108->host). It will assert the busy pin.
3. The busy pin will fire an interrupt on the host, after which it will immediately:
    a. Process the interrupt but take no further action, as the wake pin has already been asserted and the shared host interface is currently enabled/initialized.
4. After MM6108->host communication completion, hardware sleep will be initiated as described above.

5 Electrical Characteristics

5.1 Absolute Max ratings

Stress beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation is guaranteed for recommended operating conditions only. Operating the device outside of recommended conditions may result in reduced lifetime and/or reliability problems, even if the absolute maximum ratings are not exceeded.

Parameter	Min	Max	Unit
VBAT voltage	-0.3	4.3	V
Voltage on digital I/O pin	-0.3	4.3	V
Voltage on analog/RF pin	-0.3	1.32	V
Storage Temperature	-40	125	°C
RF Input Power (CW)	-	6	dBm

Table 6: Absolute max ratings

5.2 Immunity

Parameter			Min	Max	Unit
Electrostatic discharge (ESD) performance	Human body model (HBM), per ANSI / ESDA / JEDEC JS001	RF Input	-500	500	V
		All pins except RF Input	-2000	2000	V
	Charged device model (CDM), per JESD22-C101	All pins	-500	500	V

Table 7: Immunity

5.3 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature (MM6108IQ)	-40	25	85	°C
V_{BAT} / V_{BAT_AON} [2]	3.0	3.3	3.6	V
VDDIO[1]	1.62	3.3	3.6	V
Digital I/O voltage	0	3.3	VDDIO	V

Table 8: Recommended operating conditions

[1]VDDIO should not exceed VBAT
[2]V_{BAT_AON} should be greater than or equal to VBAT during power-up.
Performance specifications are achieved under typical operating conditions unless otherwise specified.

5.4 Power Consumption

5.4.1 Transmit power consumption

Mode	Condition: T_A=25°C, V_{BAT}/V_{DDIO} = 3.3V	V_{BAT} Current			Unit
		Min	Typ	Max	
Transmit current (MCS7, 3 dBm, 100% D.C.)	1 MHz channel	33	43	53	mA
	2 MHz channel	39	45	52	mA
	4 MHz channel	46	52	60	mA
	8 MHz channel	56	63	76	mA
Transmit current (MCS0, 6 dBm, 100% D.C.)	1 MHz channel	43	58	76	mA
	2 MHz channel	37	47	60	mA
	4 MHz channel	45	54	62	mA
	8 MHz channel	57	67	77	mA

Table 9: Transmit power consumption

5.4.2 Receive power consumption

Mode	Condition: T_A=25°C, V_{BAT}/V_{DDIO} = 3.3 V	V_{BAT} Current			Unit
		Min	Typ	Max	
Listen	1 MHz channel	22	26	31	mA
	2 MHz channel	24	28	33	mA
	4 MHz channel	27	32	38	mA
	8 MHz channel	32	37	43	mA
Active receive MCS7	1 MHz channel	24	26	35	mA
	2 MHz channel	28	30	39	mA
	4 MHz channel	34	40	46	mA
	8 MHz channel	45	53	61	mA
Active receive MCS0	1 MHz channel	20	26	35	mA
	2 MHz channel	26	28	36	mA
	4 MHz channel	30	36	46	mA
	8 MHz channel	45	48	59	mA

Table 10: Receive power consumption

5.4.3 Sleep power consumption

Mode	Condition: T_A=25°C, V_{BAT}/V_{DDIO} = 3.3 V	V_{BAT}			Unit
		Min	Typ	Max	
Snooze	RC Oscillator on, Memory retained, configurable wake up timer	9.5	42	370	uA
Deep sleep	RC Oscillator on, configurable wake up timer	0.8	1	1.8	uA
Hibernate	Power off, wait for external interrupt	0.03	0.05	1	uA

Table 11: Sleep power consumption

5.4.4 DTIM3 power consumption

Mode	Condition: T_A=25°C, V_{BAT}/V_{DDIO} = 3.3 V, 102.4 ms Beacon Interval	V_{BAT}			Unit
		Min	Typ	Max	
S1G beacons	1 MHz channel	370	385	395	uA
	2 MHz channel	370	385	395	uA
	4 MHz channel	265	275	285	uA
	8 MHz channel	265	275	285	uA
S1G beacons with proprietary DTIM signaling[1]	1 MHz channel	170	188	200	uA
	2 MHz channel	170	188	200	uA
	4 MHz channel	165	175	185	uA
	8 MHz channel	165	175	185	uA

Table 12: DTIM3 power consumption

5.4.5 DTIM10 power consumption

Mode	Condition: T_A=25°C, V_{BAT}/V_{DDIO} = 3.3 V, 102.4 ms Beacon Interval	V_{BAT}			Unit
		Min	Typ	Max	
S1G beacons	1 MHz channel	135	140	155	uA
	2 MHz channel	135	140	155	uA
	4 MHz channel	95	105	120	uA
	8 MHz channel	95	105	120	uA
S1G beacons with proprietary DTIM signaling[1]	1 MHz channel	80	85	100	uA
	2 MHz channel	80	85	100	uA
	4 MHz channel	75	80	95	uA
	8 MHz channel	75	80	95	uA

Table 13: DTIM10 power consumption

[1] Signaling that indicates whether a power save STA should receive and process an entire beacon

5.5 RF Specifications

5.5.1 Frequency Range

The MM6108 radio operates in the frequency range from 850 MHz to 950 MHz, covering the upper sub-11 GHz band.

Region	Sub 1 GHz bands available (MHz)	Total BW available (MHz)
USA	902 - 928	26
Europe	863 - 868 917.4 -919.4	7
Australia	915 - 928	13
Japan	915.9 - 928.1	11
Singapore	866 - 869 920 - 925	8
India	865 - 868	3

Table 14: Global frequency bands

5.5.2 Receiver

5.5.2.1 Sensitivity

Sensitivities for 10% packet error rate, 1000 byte packets.

MCS index	Modulation scheme	Coding rate	Phy rate (Mbps) per BW				Minimum receive sensitivity (dBm)			
			1 MHz	2 MHz	4 MHz	8 MHz	1 MHz	2 MHz	4 MHz	8 MHz
10	BPSK	1/2 x 2	0.17	N/A			-107	N/A		
0	BPSK	1/2	0.33	0.72	1.5	3.3	-105	-103	-101	-97
1	QPSK	1/2	0.67	1.4	3.0	6.5	-102	-100	-97	-93
2	QPSK	3/4	1.0	2.2	4.5	9.8	-99	-97	-95	-91
3	16-QAM	1/2	1.3	2.9	6.0	13	-96	-94	-91	-88
4	16-QAM	3/4	2.0	4.3	9.0	20	-93	-90	-88	-85
5	64-QAM	2/3	2.7	5.8	12	26	-89	-87	-84	-80
6	64-QAM	3/4	3.0	6.5	14	29	-88	-85	-83	-79
7	64-QAM	5/6	3.3	7.2	15	33	-87	-84	-81	-77

Table 15: Receiver sensitivity

5.5.2.2 Adjacent Channel Rejection

Adjacent channel rejection is measured by setting the requested signal's strength 3 dB above the rate-dependent sensitivity and raising the power of the interfering signal until 10% PER is caused for a PSDU length of 256-byte packets. The power difference between the interfering and requested channel is the corresponding adjacent channel rejection:

Bandwidth (MHz)	MCS Index	Modulation Scheme	Coding Rate	Adjacent Channel Rejection (dB) IEEE Spec	Adjacent Channel Rejection (dB)
4	0	BPSK	1/2	16	34
	2	QPSK	3/4	11	23
	4	16-QAM	3/4	4	21
	7	64-QAM	5/6	-2	3
8	0	BPSK	1/2	16	26
	2	QPSK	3/4	11	24
	4	16-QAM	3/4	4	23
	7	64-QAM	5/6	-2	10

Table 16: Adjacent channel rejection

5.5.3 Transmitter

Note: The following transmit power levels are for IEEE compliance for 802.11ah. This does not consider any backoffs needed to adhere to regional spectrum compliance (eg, FCC, IC, TELEC).

Tx output power (1, 2 MHz BW)	Min (dBm)	Typical (dBm)	Max (dBm)
MCS 0	5.3	6.4	7.4
MCS 7	1.4	2.8	4.1

Table 17: Transmitter output

5.6 Digital Specifications

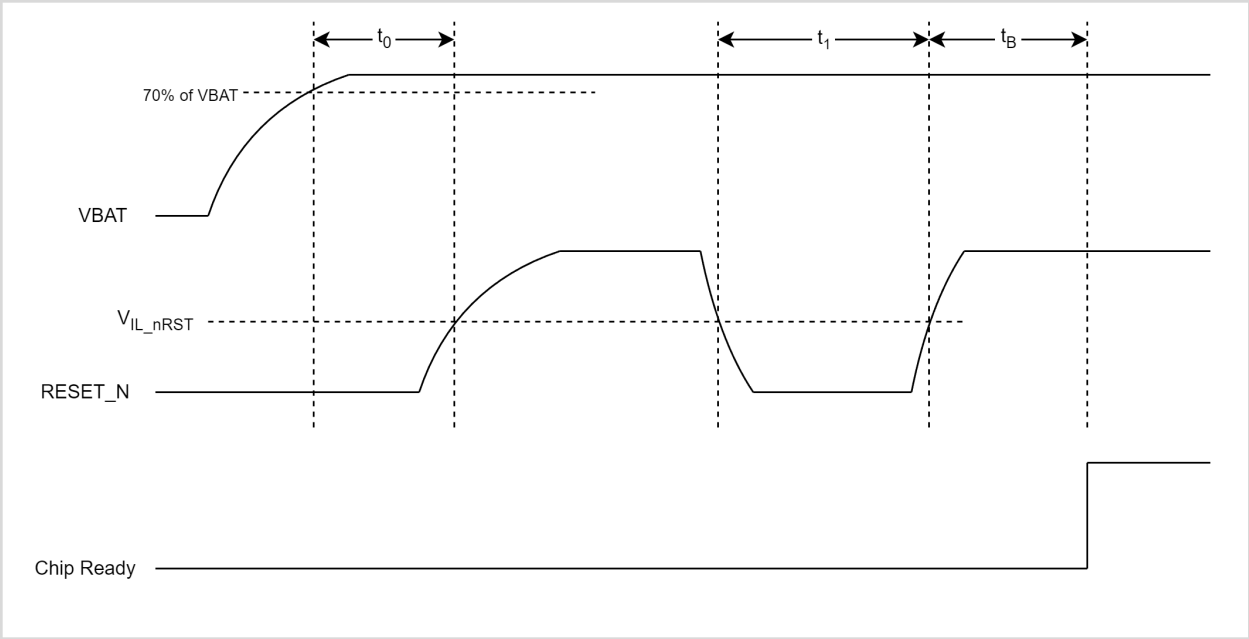


Figure 10: Powering on and reset timing diagram

Parameters	Description	Min	Max	Unit
V_{IL_nRST}	Reset threshold	450		mV
t_0	Time between VBAT brought up (3.3V) and RESET_N being activated	50		µs
t_1	Duration of RESET_N signal level < VIL_nRST to reset the chip	1000		µs
t_B	Boot Time		6	ms

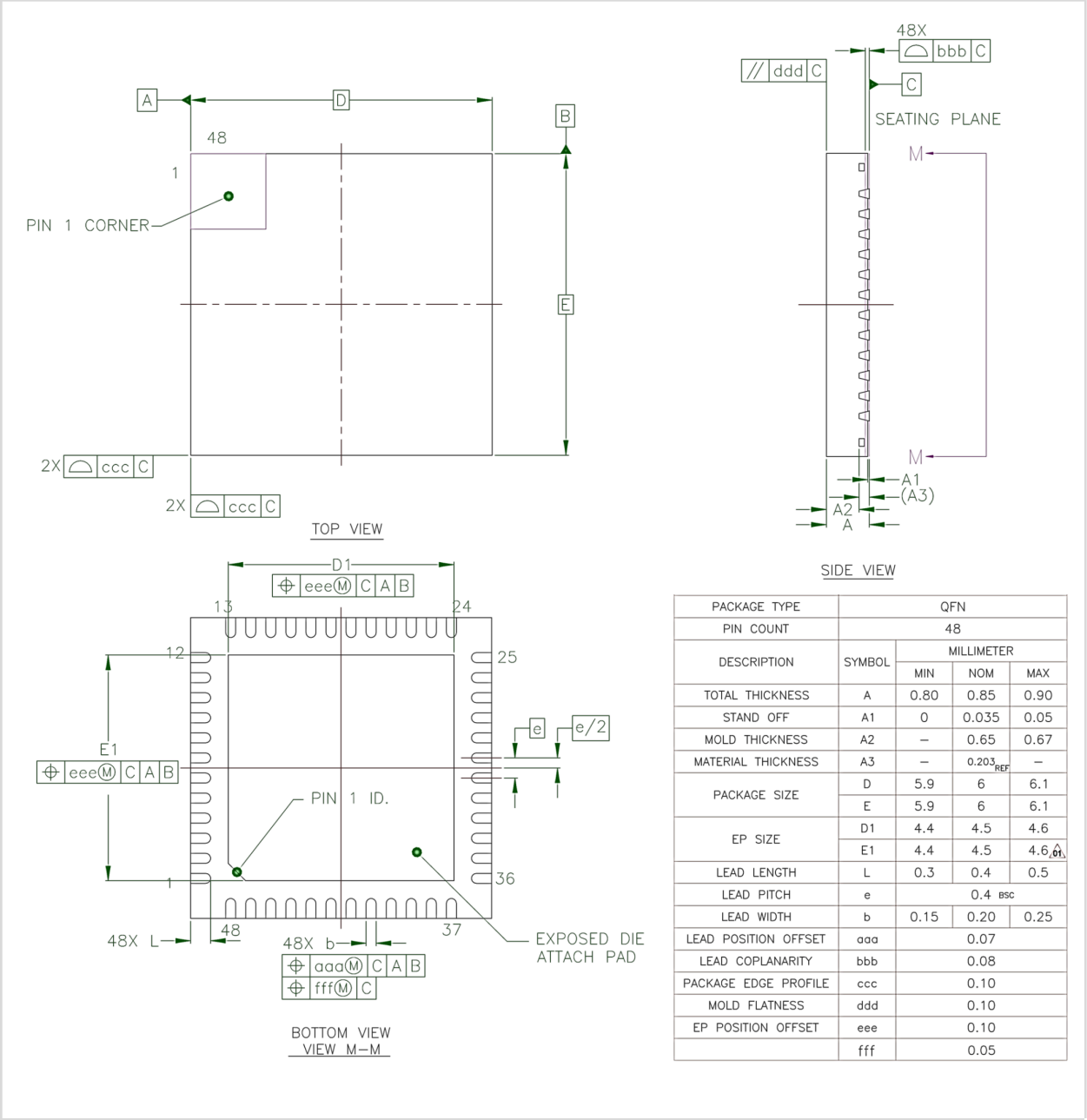
Table 18: Digital specifications

Parameters	Description	VDDIO	Min	Max	Unit
V_{IL_GPIO}	Low input threshold for all GPIO and SDIO pins	1.8	-0.3	0.63	V
		2.5	-0.3	0.7	V
		3.3	-0.3	0.8	V
V_{IH_GPIO}	High input threshold for all GPIO and SDIO pins	1.8	1.17	3.6	V
		2.5	1.7	3.6	V
		3.3	2.0	3.6	V
V_{OL_GPIO}	Low output voltage for all GPIO and SDIO pins assuming a 8mA load	1.8	0.13	0.38	V
		2.5	0.10	0.27	V
		3.3	0.08	0.18	V
V_{OH_GPIO}	High output voltage for all GPIO and SDIO pins assuming a 8mA load	1.8	1.34	1.70	V
		2.5	2.20	2.41	V
		3.3	3.07	3.23	V
V_{OL_SDIO}	Low output voltage for all SDIO pins assuming a 8mA load	1.8	0.17	0.52	V
		2.5	0.14	0.36	V
		3.3	0.11	0.24	V
V_{OH_SDIO}	High output voltage for all SDIO pins assuming a 8mA load	1.8	1.19	1.67	V
		2.5	2.10	2.39	V
		3.3	2.99	3.21	V

Table 19: Digital Specifications

6 Package Information

6.1 Package Dimensions



PACKAGE TYPE		QFN		
PIN COUNT		48		
DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	–	0.65	0.67
MATERIAL THICKNESS	A3	–	0.203 REF	–
PACKAGE SIZE	D	5.9	6	6.1
	E	5.9	6	6.1
EP SIZE	D1	4.4	4.5	4.6
	E1	4.4	4.5	4.6
LEAD LENGTH	L	0.3	0.4	0.5
LEAD PITCH	e	0.4 BSC		
LEAD WIDTH	b	0.15	0.20	0.25
LEAD POSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

Figure 11: Package dimensions

6.2 Thermal Properties

PIN	Size	Power (W)	Ta (°C)	Theta JA (°C/W)	Psi JT (°C/W)	Theta JC (°C/W)
48	QFN 6x6	1	25	31.22	0.26	15.703

Table 20: Thermal properties

Ta: ambient Temperature, defined as the temperature of the surrounding environment expressed in °C. The temperature range can be found in the recommended operating conditions section of the datasheets.

Theta JA: thermal resistance junction-to-ambient

Psi JT: thermal characterization parameter between the junction and package top.

Theta TJ: junction temperature rise over case in deg C/ Watt of chip power dissipation.

Tj = junction temperature (during operation). It is determined by P x theta JA

Notes:

- Power = power consumed by the device
- The maximum junction temperature should be controlled to less than 125oC
- The actual maximum junction temperature is determined using Theta JA, and depends on ambient temperature as well as power dissipation in the actual use.

JEDEC standards can be found at www.jedec.org under the JESD51 standard.

6.3 IC Markings

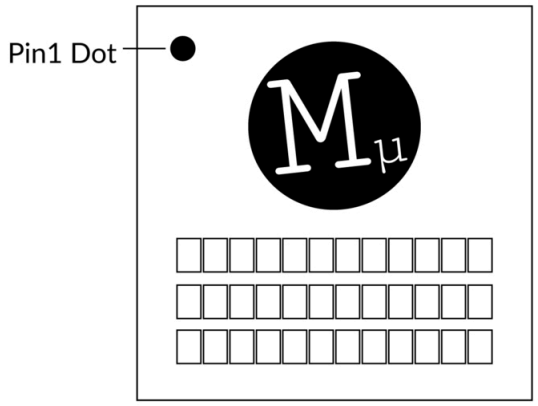


Figure 12: IC marking diagram

Line	Title	Example	Description
1	MMXXXXMDSn	MM6108MIQ	Device number; Optional: Custom Marketing Letter; Temperature Grade; Package Type;
2	TA12 YYWW	TA2103	Fab/Assembly codes; 2 digits for Silicon revision (Major, Minor - Internal Only); date code YYWW;
3	XXXXXXX	MOR946N001	8 digits Assy Lot number;

Table 21: IC markings

* All Morse Micro ICs are lead-free

Line	Title	Example	Description
1	Major silicon revision	0..9	Designated by a single number from 0 to 9
2	Minor silicon revision	0..9	Designated by a single number from 0 to 9
M	Custom Marketing suffix	M, L	M: 56 pin package (“Medium”) L: 64 pin package (“Large”)
D	Temperature Grade	I/C	I = -40°C to 85°C; C = 0°C to 70°C
S	Package Type code	Q/B	Q: QFN; B: FCBGA/BGA
n	Bond-Out Option	0..9	Designated by a single number 0..9

7 PCB Land Pattern

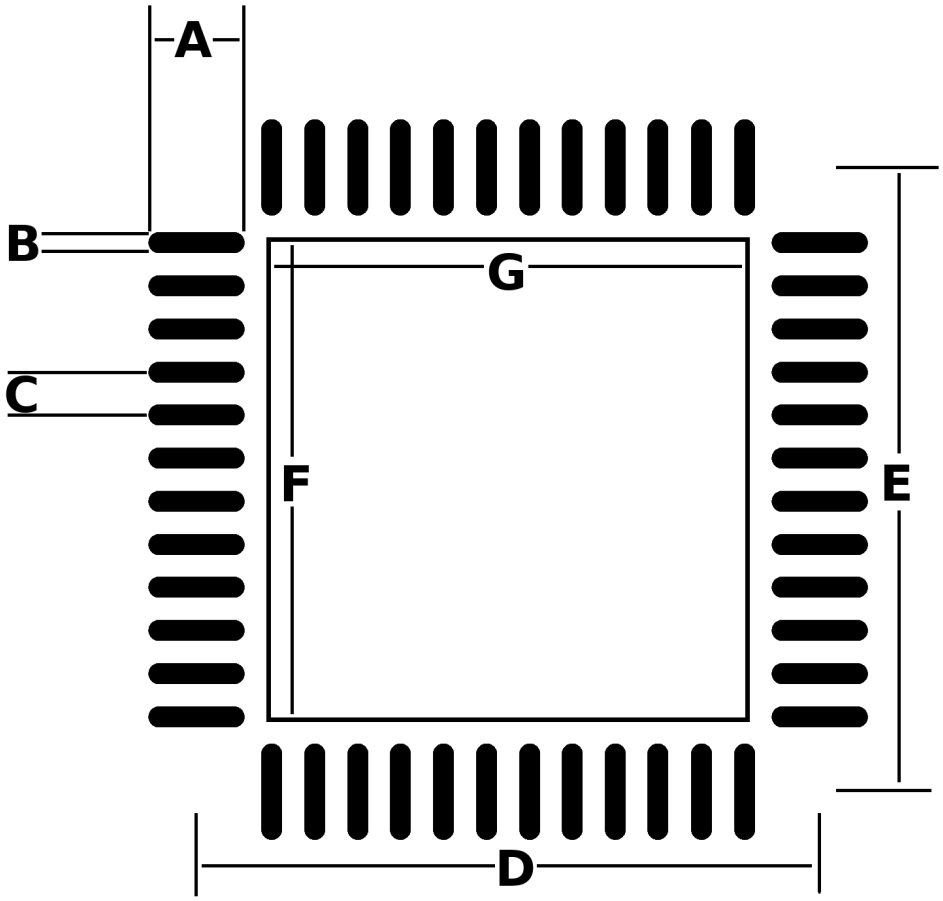


Figure 13: PCB land pattern diagram

Key	Dimension (mm)
A	0.90
B	0.20
C	0.40
D	5.80
E	5.80
F	4.50
G	4.50

8 Solder Stencil Pattern

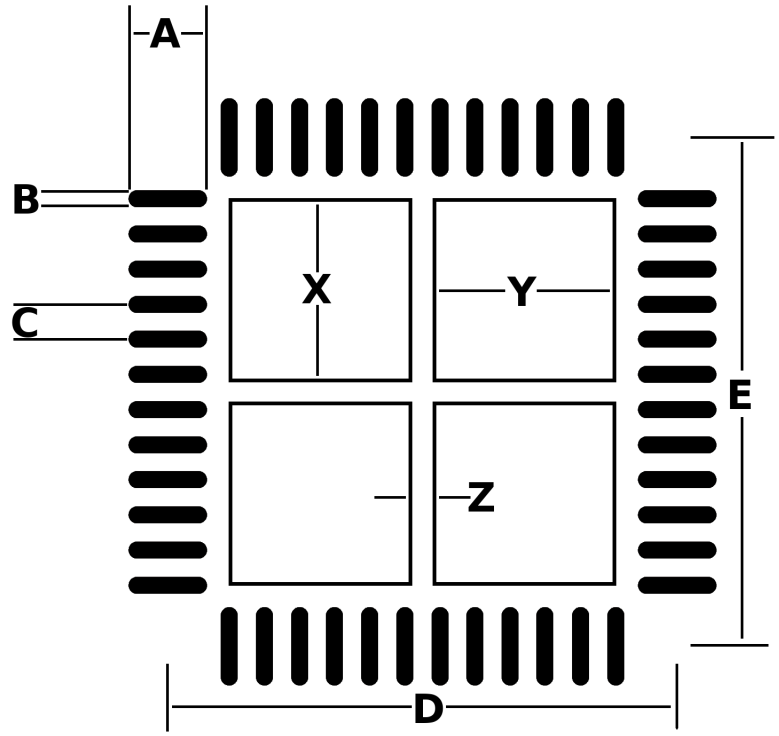


Figure 14: Solder stencil pattern diagram

Key	Dimension (mm)
A	0.80
B	0.15
C	0.40
D	5.80
E	5.80
X	2.00
Y	2.00
Z	0.50

9 Recommended Soldering Profile

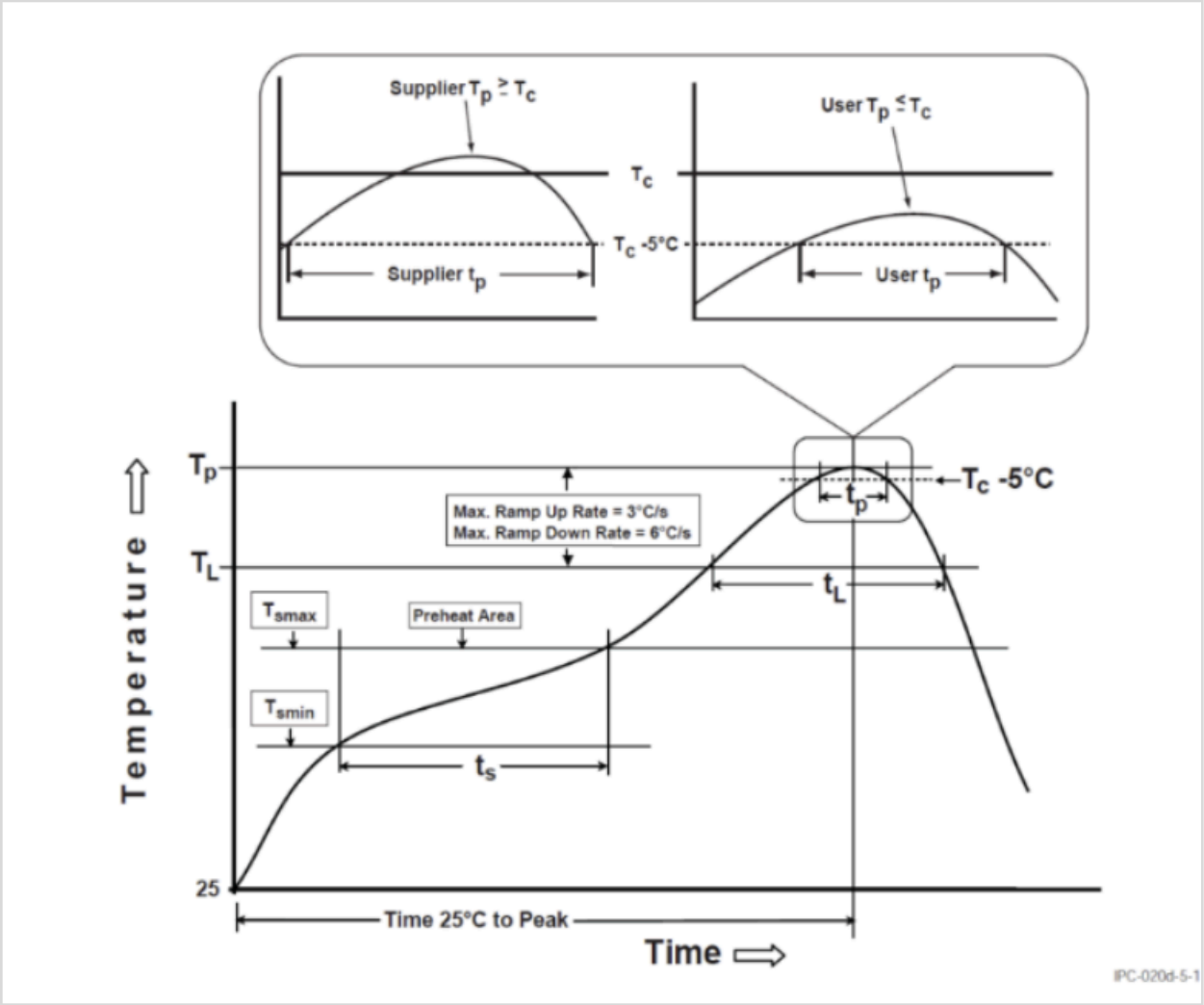


Figure 15: Soldering Profile

Pb-free (SAC Alloys) Process - Classification Temperature (TC)

Package Thickness	Volume (mm^3)		
	< 350	350 - 2000	> 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
> 2.5 mm	250 °C	245 °C	245 °C

Table 22: Soldering profile

Profile Feature	Pb-free Assembly
Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	150 °C 200 °C 60-120 seconds
Ramp-up rate (TL to TP)	3 °C/second max.
Liquidus temperature (TL) Time (tL) maintained above TL	217 °C 60-150 seconds
Peak package body temperature (TP)	For users TP must not exceed the Classification temp in Table 4-2. For suppliers TP must equal or exceed the Classification temp in Table 4-2.
Time (tP)* within 5 °C of the specified classification temperature (TC), see Figure 5-1	30* seconds
Ramp-down rate (TP to TL)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), TP shall be within +/- 2 °C of the live-bug TP and still meet the TC requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if TC is 260 °C and time tP is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Producers or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification is desired.

10 Packaging and Labeling

10.1 Tape & Reel Specification

Term	Definition
Product	MM6108
# Units	3,000
Reel Size	13 inches
Pizza Box	Yes
Vacuum Seal	Yes
Dry Bake	125 °C / 24 hours (MSL3)
Reel Pocket Dimensions	Refer to Figure 2
Pin 1 indicator	Marked on the chip

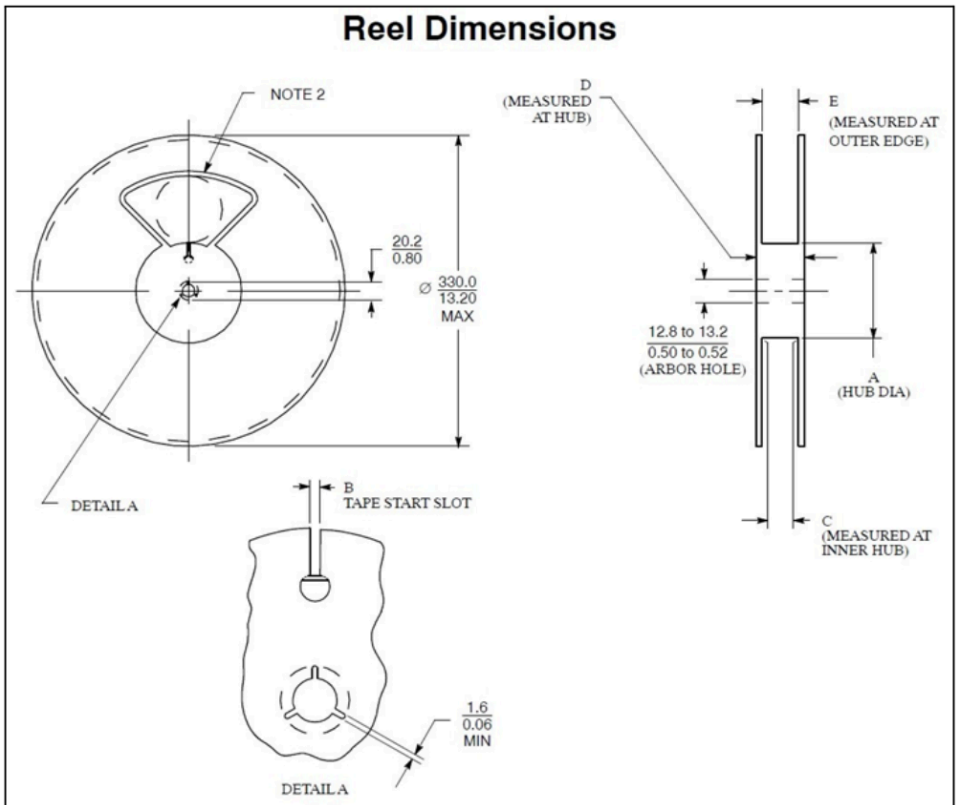
Table 23: Tape and reel specifications

10.2 Tray Specification

Term	Definition
Product	MM6108
# Units	490
Tray Size	322.6mm x 135.9mm
Pizza Box	No
Vacuum Seal	Yes
Dry Bake	125 °C / 24 hours (MSL3)
Pin 1 indicator	Marked on the chip

Table 24: Tray specifications

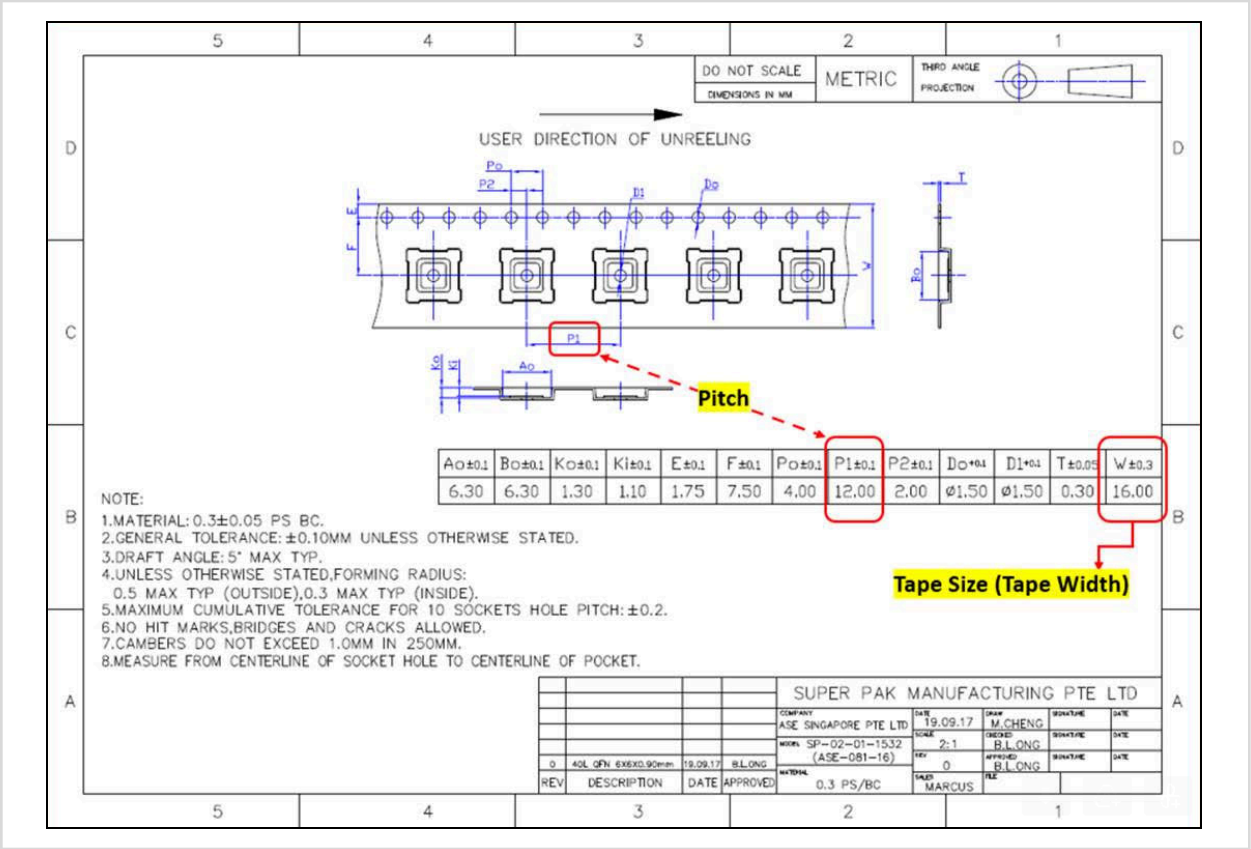
10.3 Reel Dimensions



Reel Diameter	Tape Size	A mm (inches)		B mm (inches)		C mm (inches)		D (Max)	E (Max)
		Min	Max	Min	Max	Min	Max		
178.0 (7.01)	16.0 (0.63)		50.0 (1.97)	6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)	178.0 (7.01)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	56.0 (2.20)	150.0 (5.91)		10.0 (0.39)	11.0 (0.43)	56.4 (2.22)	58.4 (2.30)	62.4 (2.46)	59.4 (2.34)
330.0 (12.99)	44.0 (1.73)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	44.4 (1.75)	46.4 (1.83)	62.4 (2.46)	47.4 (1.87)
330.0 (12.99)	32.0 (1.26)	100.0 (3.94)		10.0 (0.39)	11.0 (0.43)	32.4 (1.28)	34.4 (1.35)	38.4 (1.51)	35.4 (1.39)
330.0 (12.99)	24.0 (0.94)	60.0 (2.36)		9.5 (0.37)	10.5 (0.41)	24.4 (0.96)	26.4 (1.04)	30.4 (1.51)	27.4 (1.08)
330.0 (12.99)	16.0 (0.63)			6.5 (0.26)	7.5 (0.30)	16.4 (0.65)	18.4 (0.72)	22.4 (0.88)	19.4 (0.76)
330.0 (12.99)	12.0 (0.47)			4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.01)	12.0 (0.47)	50.0 (1.97)		4.5 (0.18)	5.5 (0.22)	12.4 (0.49)	14.4 (0.57)	18.4 (0.72)	15.4 (0.61)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		2.5 (0.10)	3.5 (0.14)	8.4 (0.33)	9.9 (0.39)	14.4 (0.47)	10.9 (0.43)
330.0 (12.99)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)
178.0 (7.00)	8.0 (0.31)	50.0 (1.97)		4.0 (0.16)	5.0 (0.20)	8.4 (0.33)	9.9 (0.39)	14.4 (0.57)	10.9 (0.43)

Figure 16: Reel dimensions

10.4 Tape and Device Placement Dimensions



Ao±0.1	Bo±0.1	Ko±0.1	Ki±0.1	E±0.1	F±0.1	Po±0.1	P1±0.1	P2±0.1	Do+0.4	D1+0.4	T±0.05	W±0.3
6.30	6.30	1.30	1.10	1.75	7.50	4.00	12.00	2.00	ø1.50	ø1.50	0.30	16.00

Figure 17: Tape and device placement dimensions

11 Handling and Storage

The MM6108IQ IC is a moisture-sensitive device rated at Moisture Sensitive Level 3 (MSL3) per IPC/JEDEC J-STD-20.

After opening the moisture-sealed storage bag, modules that will be subjected to reflow solder or other high-temperature processes must be:

1. Mounted to a circuit board within 168 hours at factory conditions (≤30°C and <60% RH)
   OR
2. Continuously stored per IPC/JEDEC J-STD-033

ICs exposed to moisture and environmental conditions exceeding packaging and storage conditions MUST be baked before mounting according to IPC/JEDEC J-STD-033. Failure to meet packaging and storage conditions will result in irreparable damage to modules during solder reflow.

12 Part Number and Ordering Information

Part Number	Packing Type	MOQ	Package	Description	Operating Ambient Temperature
MM6108IQ-T	Tray	490	QFN 6x6	IEEE 802.11ah Sub-1 GHz 1/2/4/8 MHz Wi-Fi HaLow SoC	-40°C to 85°C
MM6108IQ-TR	Tape & Reel	3000			

Table 25: Part number and ordering information

13 Revision History

Release Number	Release Date	Release Notes
DS104	17 Jun 2025	Updated formatting
DS103	15 Dec 2023	Added power sequencing requirements Added Vih, Vil, Voh, and Vol specifications Added solder profile Added packaging Added chip markings Added sleep/wake pin sequencing
DS102	8 Apr 2022	Updated table 5.5.1 RF Spectrum Range Added PCB land pattern and solder stencil Updated electrical characteristics Added Max/Min values
DS101	4 Nov 2021	Updated recommended operating conditions Updated Tx and Rx power consumption Updated Adjacent Current Rejection
DS100	1 Jun 2021	Initial release

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